



# ADRES PROCESSOR

ADRES is a processor architecture designed for next-generation mobile terminals. ADRES processors combine excellent power efficiency, performance, and flexibility. Through an XML template, designers can create the ADRES processor instance that is best suited for their applications. Applications for ADRES processors can be completely programmed in a high-level programming language (C).

## MOBILE MULTIMEDIA: MULTI-MODE SCENES CALL FOR PROGRAMMABLE PLATFORMS

Tomorrow's mobile companion should offer the user a variety of multimedia services, with broadband wireless connectivity in many different environments. Indeed the 'anything, anytime, anywhere' concept calls for multi-mode support both at the services and at the radio level. Programmable platforms hosting embedded processors can provide low-cost yet very flexible solutions to realize this paradigm.

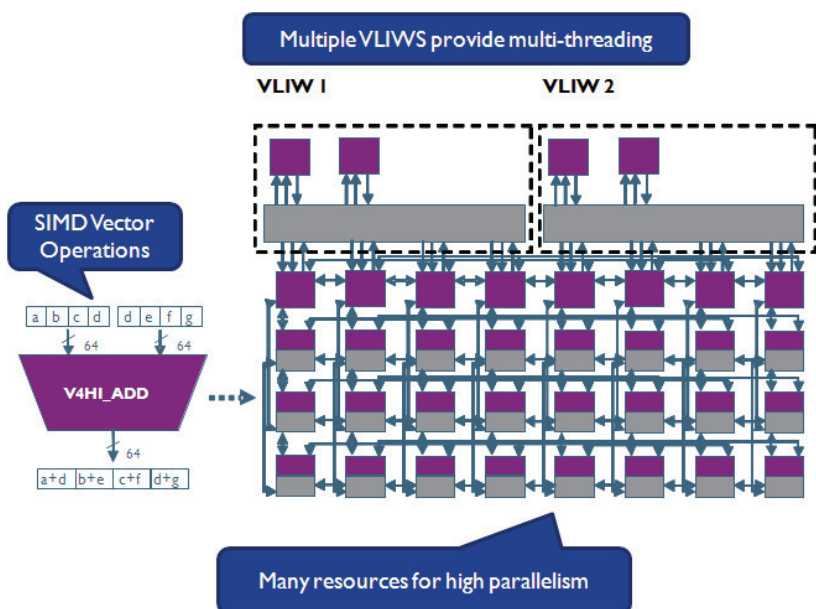
For this purpose, imec has made the ADRES (architecture for dynamically reconfigurable embedded systems) processor. The architecture achieves a high performance through the combined exploitation of different classes of parallelism, while being thoroughly optimized to meet energy consumption constraints of battery-powered devices. It comes with a tool suite that enables efficient exploration, C-compilation, and parallelization. The architecture can be tuned to meet both multimedia applications and (wireless) communication requirements.

## ADRES ARCHITECTURE TEMPLATE: FINETUNE THE INSTANCE TO FIT YOUR NEEDS

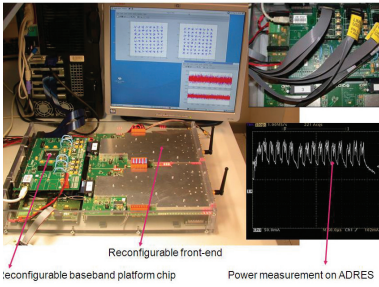
The ADRES consists of a tightly coupled very long instruction word (VLIW) processor and a coarse-grained reconfigurable array (see figure 01). ADRES is a flexible template to generate concrete instances. Together with a retargetable simulator and ANSI-C compiler, this tool chain allows architecture exploration and development of application-domain specific processors.

Key features:

- ▶ high performance thanks to multiple levels of parallelism:
  - instruction-level parallelism
  - multi-threading support
  - vector instructions support
- ▶ extremely low power by avoiding central components and through optimization of functional units, and data and instruction memory
- ▶ C-programmable



01  
ADRES processor architecture exploits many parallelism options.



02 1<sup>st</sup> generation ADRES operational in wireless prototype.

## A PROVEN SOLUTION FOR NEXT-GENERATION WIRELESS

A first-generation ADRES processor has been designed in 90nm CMOS, and integrated on a reconfigurable radio platform chip. This chip has been successfully integrated in a wireless prototype, as shown in figure 02. The technology has been validated, and power measurements were performed in various transmission and reception scenarios, which confirmed the simulated results.

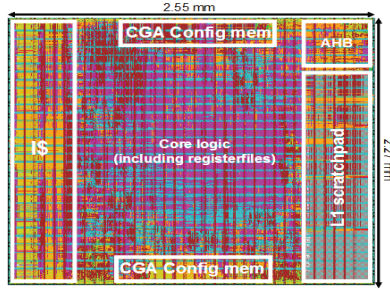
## NEW ADRES GENERATIONS SHRINK TO $\leq 40\text{nm}$ CMOS, GROW IN PERFORMANCE/ENERGY

Addressing the need for higher performance and better energy efficiency in future wireless connectivity, imec has created new generations of ADRES processors. Indeed the DSP requirements in wireless systems are growing drastically due to the increasing data rates to be supported (up to Gbit/s) and the growing complexity of the transmission schemes (especially to support MIMO (Multiple-Input Multiple-Output) systems with ever more antennas). In order to upgrade the performance, ADRES has been extended with multi-threading features and parallelization tool support.

## MORE INFORMATION

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03 40nm G silicon virtual prototype 4x4 ADRES instance (25.6 GOPS @ 400MHz).

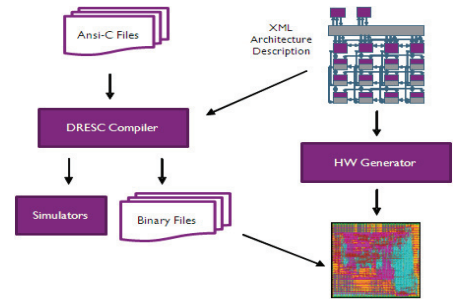
Many different optimizations have lead to a 3X better energy efficiency. Extensions to very wide SIMD will further improve the performance/power. A dedicated instruction set results in an instance particularly suited for 4G radios. While ADRES is up-scaled for the next-generation of applications, it is down-scaled to the next-generation of CMOS technologies. The architecture has been adapted to exploit the benefits of newer technologies while avoiding the drawbacks (e.g. by reducing the interconnects). A 'virtual silicon prototype' proves that high performance is reached with very nice area and power (see figure 03).

## TOOL SUITE SUPPORTS EFFICIENT EXPLORATION, COMPILATION AND PARALLELIZATION

ADRES is supported by the DRESC tool suite (see figure 04), which includes:

input:

- ▶ an XML architecture template, to describe the specific hardware instance of ADRES chosen by the designer. The designer can fully select the VLIW and CGA matrix configuration; including the array-matrix size, the functional units (FU), the type of FU connectivity, either local data or instruction registers, ...
- ▶ C-code input for the algorithm that needs to be compiled



04 Toolflow supports C-programming and architecture exploration.

output :

- ▶ compiled machine code for execution on the ADRES-processor
- ▶ a simulator for cycle-accurate simulation
- ▶ a synthesizable VHDL file for ASIC-design

Recently, the DRESC compiler has been coupled to the MPA (Multi-Processor Assist) tool. MPA helps to explore and implement parallelization on task-level, and support the multi-threading extension of ADRES.

## AVAILABLE FOR TRANSFER, PARTNERING FOR THE NEXT-GENERATION ADRES

Imec licenses the mature ADRES-processor IP to industry in a package including:

- ▶ ADRES/DRESC development framework
- ▶ exemplary architecture (including VHDL) and reference C-code
- ▶ documentation
- ▶ training and support (including tutorial & hands-on workshop, follow-up via remote Q&A)

In its green radio program, imec partners with industrial players to design the next-generation ADRES, targeting increased performance and improved power-efficiency in deeply-scaled CMOS.