

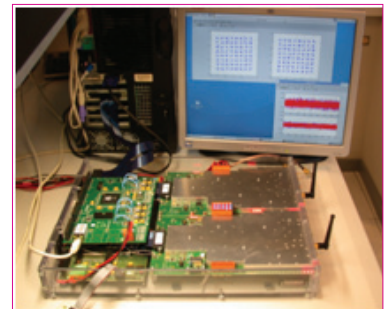


# DIGITAL BASEBAND SOLUTIONS FOR COGNITIVE RADIO

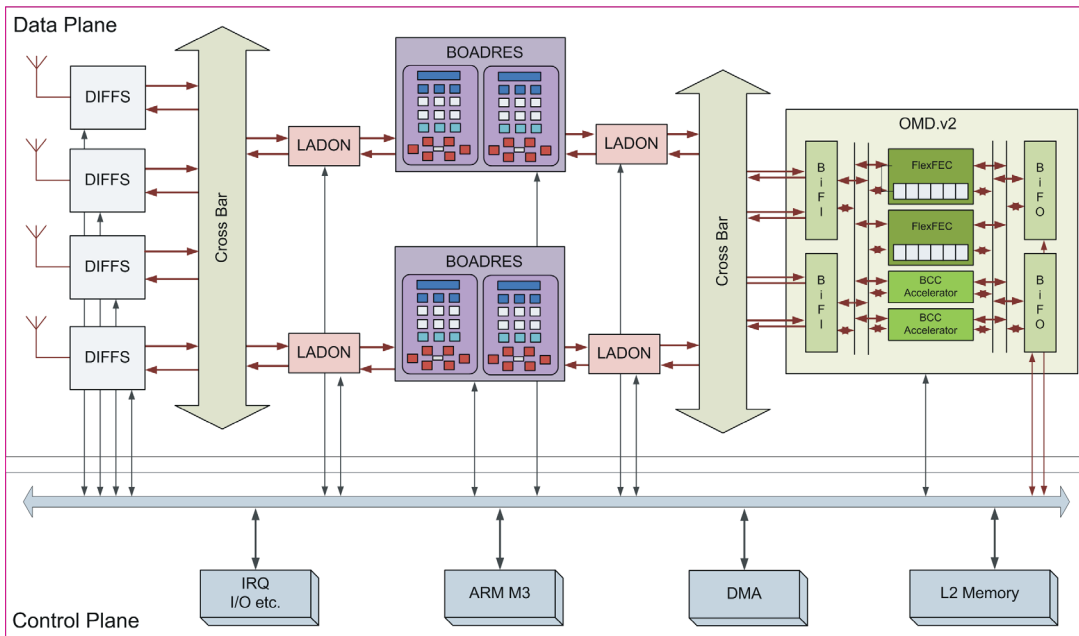
Over the last years, imec became the leading center of excellence in software-defined Radio (SDR)-technologies. This unique track record is leveraged in its continued research for next-generation cognitive reconfigurable radios. The R&D on digital baseband solutions follows a holistic approach, starting from system-level exploration, over reconfigurable platform architectures hosting innovative flexible components and suitable processors, to wireless prototypes.

## BUILDING ON EXPERIENCE: FIRST GENERATION SDR BASEBAND PLATFORM ALIVE IN WIRELESS PROTOTYPE

Imec's first generation SDR baseband platform was implemented on chip in 90G Multi-VT technology (see figure 01), and demonstrated in a wireless prototype. The platform is ready to support next-generation mobile devices, e.g. WLAN (IEEE802.11n up to 200Mbit/s), and WIMAX. The heterogeneous multi-processor system-on-chip (MPSOC) baseband platform achieves both functional flexibility and energy-efficiency through opportunistic partitioning. The platform features a DFE (digital baseband front-end) implementing the packet detection using a synchronization processor. The main data processing is carried out by two baseband processors, which are optimized instantiations of imec's first generation ADRES core.



01  
'BEAR' first generation SDR baseband implementation.



02  
COBRA platform template.

## IMEC COBRA PLATFORM TEMPLATE

The imec COBRA (COgnitive Baseband reconfigurable Radio) reconfigurable platform features the following main innovation (as indicated on figure 02):

- ▶ Novel platform architecture including upgraded interconnect for 1Gbps & concurrent streams.
- ▶ Next-generation ADRES processor with multi-threading doubles performance and energy-efficiency. Further improvements are on the roadmap.
- ▶ 'FlexFEC' processor template achieving high-speed Turbo & LDPC at low-power. Specific solutions for multi-standard broadcasting are derived.
- ▶ Novel ASIP-based digital front-end enabling flexible filtering synchronization and spectrum sensing.

## TOWARDS COBRA PLATFORM TO SUPPORT 4G AND MULTIPLE CONCURRENT STREAMS

The COBRA platform is conceived with the goal of supporting 4G requirements (up to 1Gbit/s stationary and >100 Mbit/s in full mobility), and multiple concurrent streams (e.g. allowing simultaneous digital broadcasting reception and high-speed internet access).

Specifically, the standards considered as driving applications are WLAN evolutions (IEEE802.11n to 11ac), 3GPP (LTE to LTE-advanced), and broadcasting (DVB-T/H to DVB-T2). In view of great requirements imposed by the ambitious functionality, the architecture of the platform has been upgraded with novel interconnect suited to support very high data rates, and innovative flexible components.

## KEY COBRA COMPONENTS GET SILICON PROOF

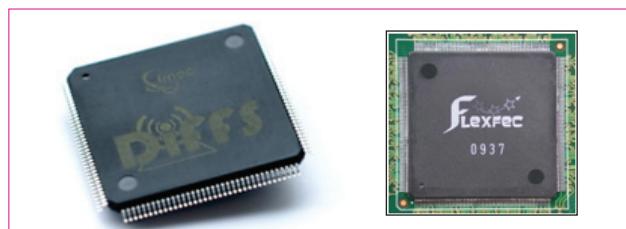
In order to check on and proof the performance and power of the key COBRA components, they are implemented on prototype chips. The Flexible FEC processor and digital front-end featuring spectrum sensing ('DIFFS') have been implemented in 65nm CMOS technology (see figure 03). Both have shown to be fully functional, and feature best-in-class power performance and area.

Next, a low power design in 40nm is on the way for the newest generation ADRES with the COBRA interconnect subsystem and controller.

## MORE INFORMATION

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03  
Silicon prototypes proof concept for COBRA components.