



VERSATILE AND FLEXIBLE SOLUTIONS FOR ADVANCED FORWARD ERROR CORRECTION

Imec offers versatile and flexible solutions for advanced Forward Error Correcting (FEC) coding, targeting data transmission applications that need to combine high-throughput and low power consumption. Imec's solutions build upon an innovative scalable and C-programmable architecture. A specific instance of the codec was proven in silicon.

KEY FEATURES

- ▶ Flexible to support both TURBO and LDPC-coding
- ▶ C-compiler support to implement new modes on the ASIP-based component
- ▶ Multi-channel operation over different modes
- ▶ Highly flexible in terms of block-size, code-rate and modulation types
- ▶ Support all interleavers or parity check matrix from the targeted applications

UNIFIED DECODER ARCHITECTURE

A patented decoder architecture provides several degrees of throughput/area scalability. The SIMD-width (n) is made flexible to vary the amount of MAP windows or LDPC check equations operating in parallel. The number of background memory banks (M) can be scaled to vary the amount of accommodated decoding threads. The number of used SIMD-processors can be changed to pipeline turbo/LDPC-blocks, iterations or (LDPC-) layers.

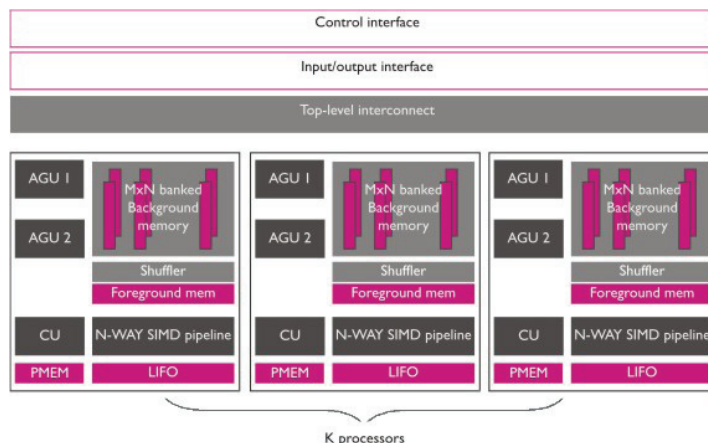
template can also be used to specify application-specific FEC instances with specific throughput or performance requirements in a quick way. A variety of applications includes but is not limited to:

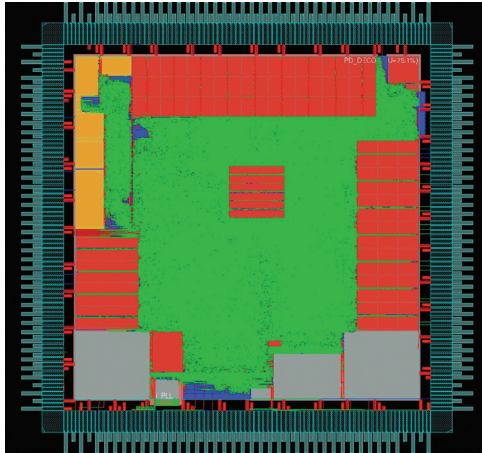
- ▶ 3rd generation mobile phones (3GPP/LTE can be supported incl. cat 5)
- ▶ Wireless networks (IEEE802.11n, IEEE802.11ac, IEEE802.16(e)) up to Gbit/s rates
- ▶ Television broadcasting (DVB-S2/T2, CMMB)
- ▶ Digital Video Broadcasting - Satellite services to Handhelds (DVB-SH)

APPLICATIONS

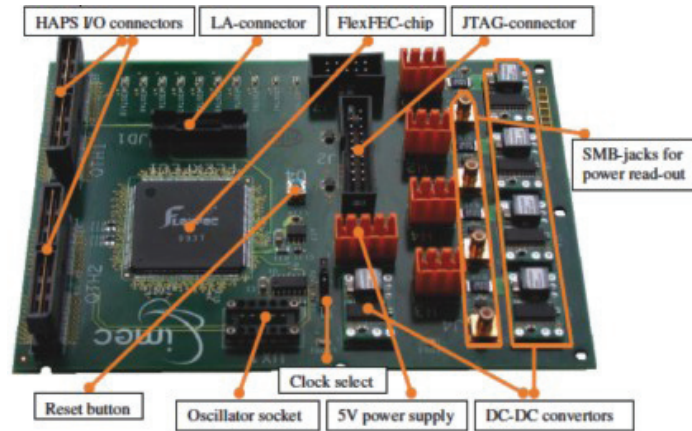
The unparalleled flexibility allows chip makers to build multi-mode FEC engine instances starting from a template design database resulting in area savings. This

The specific template, supporting both turbo and LDPC-decoding can be pruned aggressively in case of LDPC-decoding only, leading to substantial savings in area and power consumption.

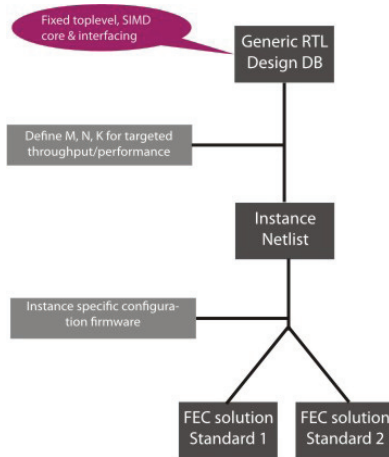




03 Flexible FEC chip instance layout view.



04 Flexible FEC chip embedded in test PCB.



05 Instantiation flow.

SILICON PROVEN TECHNOLOGY

A template instance capable of supporting WiFi (802.11n), WiMax (802.16e) and 3GPP/LTE standard was implemented in a commercial 65nm CMOS technology. Next to the flexible decoder architecture, a configurable turbo and LDPC-encoder was added. The chip was mounted onto a test-PCB which is connected to a FPGA-board allowing verification of all supported modes. Innovative upgrades and optimizations have been worked out which increase the throughput significantly (up to Gbit/s) while lowering the power consumption.

AVAILABILITY

Imec licenses this IP to industry in a package including:

- ▶ Specification documentation (including MATLAB reference code for typical Turbo and LDPC-codes)
- ▶ Design database:
 - Un-encrypted and suitably commented RTL source code + simulation environment
 - System C simulation with bit-exact correspondence to RTL behavior
 - Firmware for LDPC and CTC
 - Test vectors and test benches for RTL and C
- ▶ User guide
 - How to build specific instantiations?
 - How to write firmware for FlexFEC architecture?
- ▶ Specific instance final netlist & samples
- ▶ C-compiler
- ▶ Hands on training

MORE INFORMATION

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