ULTRA-LOW-POWER DIGITAL SIGNAL PROCESSING

To increase the autonomy of today’s wireless sensor nodes, imec is developing ultra-low power digital signal processing techniques, architecture and devices. These allow reducing the amount of data to be transmitted wirelessly in exchange of more local signal processing, paving the way to autonomous wireless sensor nodes.

APPLICATION FIELDS

Highly miniaturized and autonomous sensor systems or in short wireless sensor nodes (WSN) can serve many application domains for an ambient intelligent future such as:

- Health and lifestyle (e.g. patient monitoring);
- Structural monitoring (e.g. predictive maintenance);
- Automotive (e.g. tire pressure monitoring system);
- Logistics (identification, food and pharma monitoring).

SCOPE

The autonomy of today’s wireless sensor nodes is seriously hampered by their limited intelligence and their power consumption. Typical systems use small processors or microcontrollers that can only perform elementary processing such as filtering or data encoding before they forward the information over a wireless link to a basestation or another sensor node.

We are developing ultra-low-power (ULP) signal processing techniques, architectures and devices. These will allow reducing the amount of data to be transmitted wirelessly and add intelligence to the sensor nodes, in exchange of and allow for more local signal processing. As power consumption is reduced and local decision making enhanced, this helps to increase the autonomy of the nodes.

The program aims at reducing power consumption of sensor nodes to increase their autonomy and to add intelligence. We focus on biomedical signal processing, wireless baseband and industrial process control algorithms. The envisaged solution adds a sophisticated Ultra-Low-Power (ULP) DSP to the sensor node architecture. The DSP will be implemented in a state-of-the-art low-power CMOS process leading to a power efficiency of several hundred MOPS/mW.

ACTIVITIES

- Scalability;
- Power management;
- Ultra-low-power memories, memory hierarchies and data paths;
- Low voltage circuit design;
- Power-aware instruction set processor architectures;
- Customized and reconfigurable instruction-sets for ultra-low-power;
- Domain specific algorithms for ultra-low-power.

The design is supported by a rigorous methodology that allows making derived architectures and their corresponding software tools in a systematic way.
MORE INFORMATION

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POTENTIAL PARTNERS

Partners joining this research program get access to the prototype ICs, system studies, simulation models and underlying patents. Currently we offer:

- Ultra low power BioDSP, a processor designed for biomedical signal processing and enabling continuous CWT ECG processing at 57 microWatt and 8 channel EEG processing at 250 microWatt.
- Ultra low power BioFlux, using the known and proven NXP Coolflux BSP technology for ExG biomedical processing and baseband processing. This IC has optimized memory and communication architecture and full power gating to reduce active, sleep and standby power consumption;
- A combined analog sensor readout and biomedical processing digital backend uniquely positioned to deal with ambulatory ECG processing. It can remove the motion artifacts that inherently are there with people on the move. Minimal power consumption when possible, maximal processing when needed to recompose a weak, distorted signal;
- Ultra low power, low leakage SRAM memories with leakage less than 10 microWatt and below 5Joule/access in C90nm and 65nm CMOS;
- Ultra low power implementation of PUF and AES for unique identification and encryption;
- Baseband + MAC algorithms implemented for ULP;
- Impulse UWB BB + MAC dedicated processor.

Our scientific work force is dedicated to find innovative solutions to make the partner’s product a success in the market.

This research is carried out in the framework of Holst Centre, an open innovation initiative set-up by imec and the Dutch research institute TNO.

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