IMEC prominently present at this year’s Design Automation & Test in Europe

DATE 2002, 4-8 March, Le Palais Des Congrès, Paris, France

The 5th DATE conference and exhibition is the main European event bringing together design automation researchers, users and vendors, as well as specialists in the design, test and manufacturing of electronic circuits and systems. For the third year in a row, IMEC will participate in the conference and the accompanying exhibition.

Several technical papers will be presented at the conference, focused on design technologies and tools to develop the systems-on-chip and systems-in-a-package needed for next-generations smart networked devices.

One of the keynote speeches will be given by Prof. Hugo De Man, senior research fellow IMEC and professor at the University of Leuven, Belgium, titled “On nanoscale integration and gigascale complexity in the post .com world” (see also editorial elsewhere in this issue).

During the conference, IMEC exhibits its newly developed technologies which address the challenges that appear when designing smart networked devices: support for heterogeneity and dynamic behavior.

Two demonstrations addressing the design challenges for cost-efficient real-time MPEG-4 systems will be exhibited:
• Platform-independent real-time MPEG-4 decoder
• MPEG-4 on ACUNIA’s XINGU™ 8000 platform

Both demonstrators were developed using IMEC’s ATOMIUM suite. ATOMIUM is a set of cooperating CAD tools that addresses data transfer and storage aspects for data-intensive multimedia applications.

IMEC program to push 193nm lithography to the ultimate limits

IMEC announces a continuation of its 193nm lithography Industrial Affiliation Program (IIAP) on a high NA 193nm step-and-scan system to push 193nm lithography beyond 100nm.

In 1999, IMEC started an IIAP on 193nm lithography using the first ASML PASS500/900 full-field step-and-scan system (maximum NA of 0.63), to accelerate the introduction of 193nm technology. This program was focused on the first critical lithography levels of 130nm and 100nm CMOS technology. The development of these technologies is currently ongoing on this system.

Today, it has become clear that 193nm lithography will be introduced in volume manufacturing for the 100nm technology node but will also be pushed beyond 100nm, using new generation step-and-scan systems equipped with a higher NA lens. Still, a lot of development work is needed to push 193nm beyond 100nm.

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In the past decade, PC and Internet gave rise to the com world. With the current progress of sub-100nm technology, DSP, MEMS technology, RF CMOS and nanoelectronics which rapidly merge with biotechnology, we are now entering the post PC and post com era. We are evolving towards a smart environment (ambient intelligence) in which we will be surrounded by smart things that communicate with each other and thereby augment our consciousness, protect our health and globally connect people and things. The driving force will no longer be the PC but information technology that adapts to the human being rather than vice versa.

The key to such pervasive computing is global broadband networking at all levels from the fiber optics backbone to the wireless and wireless last kilometer down to the body area network that connects the information processing device with the adaptive intelligent environment. Designing such systems differs radically from designing CPU architectures. The art will be to design a diversity of cheap, energy-efficient, yet programmable platforms that can be configured over the Internet and communicate with humans through various human interface interfaces. It will require a grand convergence of previously separated domains such as programmable/reconfigurable multi-processor architectures with embedded software, broadband radio, MEMS and biosensor interfaces.

Technologically speaking, it will be possible to follow Moore’s curve down to the 30nm range. At this point, chips will contain 2 billion logic transistors or the equivalent of 1000 programmable processors embedded in a reconfigurable network and 50Mbyte of storage. However, design technology is confronted with gigascale complexity. The real bottleneck will not be process technology itself but in our ability to design products and services into such huge multiprocessor architectures on a single piece of silicon or in a single package.

The era of artificial intelligence or pervasive computing is based on devices that interact in an intelligent way with the human being. These devices have to feel, sense... or in other words “karen” and adapt to human behavior. This requires an enormous amount of computing power, which in its turn demands huge energy consumption. Therefore, battery powered battery powered devices will be battery powered future will thus be battery powered to have to be developed to keep the energy consumption at an acceptable level. Several novel energy sources will have to be exploited such as sun, light, vibrations, micro, micro fuel cells etc. Besides these novel energy sources, designers will have to implement multi-processor architectures that are 100 times more energy efficient than today’s CPUs.

IC complexity grows faster than the integration capabilities of new processes. Within a few years, this will result in ICs with peripheral wire bonds on a pitch of only 40µm. This goes beyond the traditional laminate and elastic interconnection technologies, which are limited to minimum pitches of 100µm. The evolution of VLSI technology also asks for an increasing bandwidth of the interconnects between ICs and other system elements. To keep up with the increasing speed and density requirements, thin-film multi-chip modules will have to be used more and more. By using 3D stacking, the interconnectio lines can be kept short.

IMEC’s novel ultra-thin chip stacking (UTCS) technology achieves a much higher 3D wiring capability than existing technologies. The UTCS structure embeds ICs that are thinned down to 10-15µm inside the multi-layer thin-film structure. To the traditional interconnects ICs can be stacked on top of each other. Novel methods were developed to connect standard commercial CMOS chips down to 10-15µm and to transfer them to the UTCS substrates.

Traditional 3D interconnect schemes connect the different layers of ICs, which greatly limits the interconnection density in the third dimension. In this new UTCS structure, via connections in the third dimension can be realized in the same area. Since these thin-film vias can be created with pad sizes smaller than 50µm, a very high interconnection density in the third dimension is obtained. The main interconnecting wire in the UTCS stack is the vertical “channel” from the CPU to the UTCS substrate. Different UTCS stacks were developed. To realize high-density connections between the metal layer below the die and the metal layer on top of the die, a special high aspect ratio vias structure was used. The method resulted in high yield via connections with diameters as small as 15µm and 50µm thick BCB layer. For standard photo-BBC via connections, a via density well above 100 vias/mm² was achieved.

Multi-processor architectures already exist from way back. The new challenge is now to make them adaptable to the human behavior. Therefore, they have to be made reconfigurable by software that is distributed over the network. This will cause a paradigm shift in the CAE world. High performance as embedded software will have to be developed together with the multi-processor architectures it will run on and this under extreme low-energy constraints.

One of the major bottlenecks with energy consumption is the transfer of data from the memory to the CPU. Currently, most designs are written in software like C++, Matlab, etc. without taking into account the optimal implementation. So far, standard optimization only gets started at a high level without knowing the architecture. Instead of writing codes as a sequence of function calls, task-communication management, and distributed storage and computation can already result in a decrease in power consumption. Once the architecture is defined, further optimization can be performed. Until now, there are no CAD tools commercially available to make such power-efficient designs.

Application targets for ATMOPUM include real-time multimedia systems, sensor networks and SoC chips. This requires a multi-disciplinary approach whereby not tools but engineering skills will be crucial. Creation of teams of system and service designers, system-on-chip architects and IP providers will be of utmost importance. Computer-aided design will be as essential as technical knowledge. This creates challenges in research, education and training. Especially universities and research institutes will have to perform concurrent research and education to have the necessary engineering talent available to exploit the potential of the oncoming technology.

This will demand a systematic methodology including HDL synthesis, behavioral synthesis, system simulation, integrated simulation, high level performance estimation and systematic refinement techniques. One of the major contributions of OCAP-x is the unified HW/SW co-simulating environment. A very high interconnection density in the third dimension is obtained. The main interconnecting wire in the UTCS stack is the vertical “channel” from the CPU to the UTCS substrate. Different UTCS stacks were developed. To realize high-density connections between the metal layer below the die and the metal layer on top of the die, a special high aspect ratio vias structure was used. The method resulted in high yield via connections with diameters as small as 15µm and 50µm thick BCB layer. For standard photo-BBC via connections, a via density well above 100 vias/mm² was achieved.

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IMEC developed a novel 3D interconnection technique for very high bandwidth interconnects between ICs. The technique is particularly interesting for high pin count dies with small pad pitches that require a high degree of interconnectivity. The method features a much higher wiring capability as compared to other 3D techniques.

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Novel 3D interconnection technique: ultra-thin chip stacking
World record: GaAs solar cells with an efficiency of 24.5%

IMEC together with its associated laboratory IMEC from the Ghent University and Umicore have realized a GaAs solar cell on a Ge substrate with a world-record efficiency of 34.5%, using a new and solar MOCVD (Metal-Organic-Crystal-Vapour Deposition) process.

IMEC has collaborated in developing the heteroepitaxial growth processes for deposition of various III-V materials on their Ge substrates. The design, processing and characterization of the solar cells were performed by IMEC. This collaboration has recently resulted in the realization of a 2x2cm² single-junction GaAs solar cell on Ge substrate, exhibiting a conversion efficiency of 24.5% under the AM1.5 solar spectrum. Up to now, the highest efficiency ever reported in literature for this type of cell was 24.3 ± 0.7%.

The epitaxial layers of the solar cell were grown using the alternative As precursor TBAs (Tributyltin Arsenic) instead of the commonly used but extremely toxic AsH₃. TBAs is less hazardous and has a much lower vapour pressure than AsH₃, leading to a much safer MOCVD process. In addition, TBAs has a considerably higher cracking efficiency, resulting in a lower consumption of source materials and a drastic reduction of toxic waste.

The excellent solar cells realized by IMEC demonstrate that switching to a safer fabrication process is possible without any loss of material or device performance. It is expected that, in the coming years, the MOCVD industry will be pushed to stop the use of AsH₃ in their processes, as toxicologists strongly recommend to lower the Threshold Limit Value (TLV) for AsH₃ from 50 to 3 ppb (parts per billion).

The project was financially supported by the IWT, the Flemish Institute for the advancement of scientific technological research in the industry.

IMEC Fellow Staf Borghs describes his vision on nano-electronics and shows how bottom-up nanotechnology can increase the performance of biosensors.

Nanoelectronics, top-down or bottom-up?

Nano-electronics is an emerging field of research and development dedicated to increasing the control over material structures of nanoscale size (0.1 to 100nm) in at least one dimension. Nanotechnology is also a cluster of emerging techniques from solid-state technology, biotechnology, chemical technology and scanning-probe technology that converges "top-down" and "bottom-up" to the nanoscale. Top-down refers to the increasingly precise machining and finishing of materials from the macroscopic down to nanoscopic scales, bottom-up synthesis from individual molecules or atoms. The convergence of disciplines closes the gap between classical chemistry, biology and solid-state technology and has already lead to fruitful interdisciplinary cooperation.

The bridging of the gap between bottom-up and top-down will not necessarily lead to smaller transistors but to a higher integration of functions on existing chips, where computing is only a part of the total functionality. This system-in-package approach will not only handle workloads but also deals with photons, motions, magnetic fields and molecular recognition. Cross-fertilization of different disciplines will create new ways of sensing, displaying and computing. Bottom-up nanotechnology, using self-assembling molecules, will find its first applications in biosensor systems. Major applications in molecular computing could follow in a much longer time frame.

Over the past year, IMEC started research on self-assembled monolayers (SAMs) to increase the performance of biosensors. Amongst others we studied for example thiols R₆(CH₂)₉SH on metal surfaces like platinum, palladium, copper and in more detail on gold. In this way, metal surfaces could be modified on the nanoscale. Surfaces could be made totally hydrophilic or hydrophobic or even expanded with the desired functional groups by using a few nanometers thick shell layer. By employing mixed SAMs, the surface could be tuned to the desired application. IMEC fabricated mixed SAMs for the selective immobilization of biomolecules like antibodies and antigens on a metal. They show enhanced qualities as a biological recognition layer concerning specificity and sensitivity. This demonstrates that by using the right chemistry on nanoscale, the overall performance of a biosensor can be drastically increased.
New algorithm for soft-breakdown detection in ultra-thin oxides

IMEC developed a new algorithm for accurate and robust automatic triggering for soft-breakdown (SBD) detection based on gate-current noise increase. The technique is sufficiently reliable for real-time, automatic breakdown detection during constant voltage stress.

As the oxide thickness is decreased in the sub-5nm range, oxide breakdown is one of the most threatening failure mechanisms in ICs. In addition, breakdown detection becomes problematic due to the occurrence of soft breakdown (SBD). However, accurate determination of the gate-oxide reliability is of utmost importance for the correct prediction of IC lifetime.

SBD is accompanied by an increase in gate-current noise, which can be monitored to determine the breakdown event outcome. However, classical noise monitors like the variance of current values during constant voltage stress are too sensitive to pre-breakdown events and spikes, resulting in false breakdown triggers. IMEC’s new optimized trigger algorithm avoids false triggers caused by current steps (such as pre-breakdown events) and current spikes (resulting from accidental measurement errors), by taking the median of a set of absolute values of consecutive current changes as breakdown monitor, called running median on $m_{r}$. With this breakdown monitor established, an obvious detection algorithm looks for steps of the running median as a function of stress time. However, since the noise increase is not always abrupt, a point-by-point triggering algorithm is unable to detect the jump in $m_{r}$. Therefore, along with the running median $m_{r}$, a reference running median $m_{ref}$ is constructed. This reference running median is created in an identical way as $m_{r}$ but is based on at least two times larger number of currents. Breakdown is detected when a significant difference between $m_{r}$ and $m_{ref}$ is detected. The $m_{r}/m_{ref}$ ratio determines the detection efficiency of the algorithm. For Gaussian noise, a higher $m_{r}/m_{ref}$ ratio lowers the probability of false early detections at the expense of a higher probability of overlooking a true noise increase due to SBD. A proper balance between these two probabilities should be determined for a given measurement setup by means of calibration.

This real-time detection algorithm is implemented in a computationally efficient way so that it can keep up with the stream of incoming current values from the measurement hardware. The technique assures correct automatic SBD detection in a wide range of stress conditions and various geometries. The new technique could be a candidate for future-stored soft-breakdown detection methodology, as being discussed by the JEDEC committees.

Feasibility proof for room-temperature spin

IMEC successfully demonstrated the injection of spin-polarized current in a LED. This experiment proves that spin-injection is achievable using a standard metal/insulator/semiconductor technology.

Electrons carry, besides charge, magnetic information. This information is present in the electron spin. In standard electronic device structures, an equal amount of spin-up and spin-down electrons takes part in the electric current. When ferromagnetic materials are embedded in electronic devices, the situation changes. Because of the natural imbalance in electron spin-up versus spin-down in ferromagnetic, the current coming from a ferromagnetic contact is spin-polarized. When this spin-polarized current can be injected with high efficiency at room temperature into a semiconductor structure, one can start to envisage spintronic components, such as nanodetectors that function on the spin of the carriers rather than their charge.

The magnetoelectronics group at IMEC successfully demonstrated spin-polarized current injection into the active region of a GaAs-based light-emitting device (LED) structure using a ferromagnetic metal. In the experiment, the magnetic contact consisted of a magnetic material (CoFe) on top of a very thin insulator (1 to 2nm of AlOx). The spin-polarized current in the LED was converted into circularly-polarized light emission. This circularity can be measured and results from a manipulation of the injected spins once they have arrived in the semiconductor. This measurement approach adds to the impact of the experiment, since it unambiguously shows the signature of spin-injection.

In this early stage of the development, the magnetic contact is at 80 Kelvin for reasons of detection efficiency. This is the first experimental evidence that spin-injection is achievable using a standard metal/insulator/semiconductor technology and an approach that should allow room-temperature spin-injection devices to be fabricated.

Europpractice provides low-cost IC prototyping and production in Alcatel’s advanced 0.35µm SiGe BiCMOS chip technology

Alcatel is offering Europpractice customers worldwide access to its high-speed 0.35µm SiGe BiCMOS technology for prototyping and volume production. This technology is ideally suited for RF products running up to 10GHz.

IMEC provides through the Europpractice IC Service initial technology support and call library distribution, back-end design support, prototypes and volume production with cost-effective design services, including multi-project wafers (MPW) for prototypes and volume production runs at Alcatel’s fabs in Belgium. IMEC distributes Alcatel’s libraries and EDA models worldwide, allowing customers to perform front-end design. IMEC performs back-end layout of customer netlists using advanced deep-submicron CAD tools, and submits the layout to Alcatel’s microelectronics division for manufacturing. Customers who prefer to complete their designs down to layout, receive access to Alcatel’s foundry capabilities, as well as low-cost products through IMEC’s MPW service. Alcatel’s SiGe BiCMOS technology offers, which has a TriMax of 50/80GHz at BVCEO higher than 3.6V, doubles the RF performance and this at virtually the same cost of a comparable Si BiCMOS technology. The 0.35µm SiGe technology comes with a dense and very rich telecom library. It can be used for a broad range of applications such as WLAN (wireless local area network) and optical networks where good RF performance at low cost is required.

Customers for the Alcatel technology are typically new start-ups, companies with smaller volume requirements and research groups in universities and research laboratories.
Wilfried Vandervorst, renown expert in ULSI characterization, appointed IMEC Fellow

IMEC has appointed Wilfried Vandervorst as IMEC Fellow for his exceptional scientific research in materials and component analysis, which is essential for R&D in advanced semiconductor process technologies. The IMEC Fellow nomination is granted to researchers at IMEC as appreciation for their outstanding scientific research that is internationally recognized.

After obtaining his PhD in applied science in 1983 from the Katholieke Universiteit Leuven (University of Leuven), Wilfried Vandervorst has spent his entire career doing fundamental research on the use and improvement of material characterization methods for advanced semiconductor processing. He has contributed significantly in the fields of dopant profiling, with the prime emphasis on the various fundamental aspects of Secondary-ion Mass Spectrometry (SIMS), and on carrier profiling using spreading-resistance probing and derived techniques. He also pioneered in device characterization based on scanning-probe microscopy using the patented concept of scanning spreading resistance microscopy and nanopotententiometry.

Wilfried Vandervorst is recognized worldwide as a leading authority in various aspects of ULSI characterization. He has authored or been co-author of more than 400 publications in internationally reviewed journals and conference proceedings, from which 45 were invited papers. He is also co-inventor of 12 patents.

In 1985, Wilfried Vandervorst was already awarded IMEC price for outstanding achievements for building up a materials characterization laboratory within IMEC. Through his work, IMEC became a center of excellence in materials and process characterization. Currently, Wilfried Vandervorst is Group Leader Materials and Components Analysis at IMEC and visiting professor at the Katholieke Universiteit Leuven.

Photovoltech: new IMEC spin-off to produce photovoltaic cells and modules

Photovoltech is to build a fabrication plant for photovoltaic cells and modules in Tianen (Belgium). The new production process developed by IMEC and granted in license to Photovoltech will enable photovoltaic cells to be produced from multi-crystalline silicon, at lower cost and with higher efficiency than by conventional technology.

Specialist companies such as Soltel will then incorporate the modules into application-specific photovoltaic systems that will supply electricity for the autonomous operation of telecommunication systems, weather stations, navigation buoys, road signs, electrification of houses and villages in developing countries. The systems will also be implemented in grid-connected systems, integrated in residential- and tertiary-sector buildings.

Construction of the fabrication plant should take around 18 months, and production of photovoltaic cells is scheduled to begin around mid-2003. The Tianen plant will have an annual capacity of 2.3 to 3.8 million units (6 to 9 MegaWattpeak), representing more than 10% of the European production of solar cells, and will soon be employing more than 50 people.

The investment involved comes to around 10 million euro. The stakes put up by the respective companies amount to 42.5% for Electrabel (including the Soltel stake), 42.5% for TotalFinaElf and 15% for IMEC.

Cross-sectional SEM picture of MIM capacitor, showing top plate, dielectric and bottom metal layer.

IMEC transfers and licenses its 0.18µm analog modules to Tower

Tower Semiconductor Ltd. has signed an agreement with IMEC for the technology transfer and licensing of analog modules and applicable technologies for its new fab that will produce 200mm wafers in geometries of 0.18µm and below. The agreement will expedite Tower’s development of specialized analog and mixed-signal technologies, applicable in cellular phones, RF, CMOS image sensors and similar technologies and will allow Tower to provide such services to its customers at the time of production ramp-up.

The agreement and license include local salicide modules, MIM (metal-insulator-metal) capacitors, high-ohmic poly resistors, N+ and P+ medium-ohmic poly resistors, inductors, and MOS and bipolar characterization for silicon integrated circuits.

Tower’s research and design teams will integrate the licensed technologies into advanced analog and mixed-signal capabilities, which will offer high levels of characterization. This will enable the new fab to offer foundry services to a wider variety of customers and applications. This transfer is an element of Tower’s strategy to integrate added value technologies and features to its baseline of high-density CMOS logic technology.

Cross-sectional SEM picture of MIM capacitor, showing top and bottom plate, and connection to top metal layer.

Tool to determine the effect of wafer treatments on the quality of the gate dielectric

IMEC developed a method to study the effects of Crystal-Originated Particles (COPs) on gate oxides based on artificial COPs. The technique avoids costly statistical evaluations.

COPs are surface defects that are normally present in Czochralski-grown silicon substrates. In spite of the name, they are actually pits. The size and density of the defects depend strongly on the crystal growth conditions, but are typically of the order of 150nm and 10 to 15 cm^-2. The defects cause premature breakdown of gate oxides. However, it has been observed that this effect is reduced in oxides thinner than 5nm.

A systematic study of the effects of COPs on gate oxides is complicated by the low defect density and the uncontrolled shape of the defects. Therefore, a method was developed to fabricate artificial COPs, called ArtCOPs, using an anisotropic etchant. The pits are typically 600nm x 600nm with ~110° oriented walls. MOS capacitor devices containing such ArtCOPs exhibit a sharp increase of the tunnel leakage current if the oxide thickness is 6nm or more. This is in agreement with experimental findings. Transmission electron microscopy reveals thickness variations in the top of the defects, caused by stress-induced oxide thinning and orientation-dependent oxide growth. Computer simulations of the oxidation process agree reasonably well with the experimentally observed profiles.

Using these profiles in device simulations, it is possible to separate the effects of oxide thinning from field distortion due to the sharp protrusion of the gate. It appears that field distortion due to stress-induced thinning is most significant in oxides thicker than approximately 5nm. The thinning effect is less prominent in thin oxides, while at the same time the tunneling probability becomes less sensitive to field distortion.

All the results agree with experimental results on real-life COPs. Therefore, the ArtCOPs and computer simulations form a useful tool to correlate the effect of wafer treatments to the quality of the gate dielectric, and thus avoid costly statistical evaluations.

Artificial Crystal-Originated Particle (ArtCOP) after etching.

Transmission Electron Microscope picture of the top of a ArtCOP, after fabrication of MOS devices with different oxide thickness. Clearly visible are the effects of orientation-dependent oxide growth and stress-induced oxide thinning.

IMEC Flash
IMEC’s microelectronics training center, MTC, organized for the first time a course on UML

MTC organized for the first time a practical course in the Unified Modeling Language (UML), the industry-standard graphical notation for modeling analysis and design models for object-oriented software systems.

Ingrid Moerman from IMEC’s associated laboratory INTEC at the Ghent University received the IMEC price for outstanding achievements 2001

AWARDS

Geert De Cubber received the Barco/F.W.O. award

Patents Japan

Patents USA

Patents Europe

Patents Australia

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...for her exceptional scientific contribution in the field of B.V.

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Main activities of the company

Fax or send to:
Katrien Marent
Corporate Communication Manager
IMEC
Kapeldreef 75
B-3001 Leuven
Belgium

Phone: +32 16 281 880
Fax: +32 16 281 637
E-mail: Katrien.Marent@imec.be