imec NEWSLETTER
aspire invent achieve
52
APRIL 2008

News from IMEC's APOLLO program

NEWS FLASH

IMEC reports three **ADC converters with record power efficiency**

At the 2008 International Solid State Circuit Conference, IMEC presented three ultra-low-power analog to digital converters (ADC) with record figures of merit targeting wireless SDR, 60GHz communication and sensor networks. The ADC architectures are available for product development to the industry through licensing as white box IP. IMEC's research now targets even faster ADCs with higher resolution and better power efficiency.

With its new CABS ADC architecture, IMEC improves the power efficiency of a 7bit 150Msamples/s ADC with factor 22.
IMEC developed a two-step 7bit 150Msamples/s ADC with a record figure of merit of 10fJ per conversion step. The innovative comparator-based asynchronous binary search (CABS) ADC architecture consists of a 1bit coarse ADC and digital to analog converter followed by a 6bit sub-ADC. The 6bit sub-convertor consists of a self-clocked (asynchronous) binary tree of comparators with embedded threshold. The input signal is applied in parallel to all comparators as in the case of Flash converters, but only 6 comparators are triggered by the binary search conversion. The power consumption scales linearly with the sampling rate and equals 0.89μW per MHz clock rate, resulting in a record figure of merit of 10fJ per conversion step. This is a factor 22 improvement compared to state-of-the-art ADCs with a similar number of bits and sampling speed. The ADC was fabricated in 90nm digital CMOS, and occupies less than 250x250μm^2.

Continued on page 4

News from IMEC's Biomedical electronics research

NEWS FLASH

IMEC presents **acquisition chip for ambulatory EEG systems**

At the 2008 International Solid State Circuit Conference, IMEC has shown a complete 200μW 8-channel electroencephalogram (EEG) acquisition application-specific integrated circuit (ASIC) suitable for miniaturized ambulatory EEG measurement. The ASIC meets the requirements for clinical EEG systems. Gain and filtering is programmable, making it suitable for a wide range of ambulatory EEG applications.

IMEC's EEG acquisition ASIC has eight programmable readout channels, an 11bit analog to digital convertor (ADC) to digitize the amplified and filtered EEG signals, a square-wave oscillator to generate the 1MHz clock for the ADC and a bias circuit. Next to the acquisition function, it also calibrates the readout channels and enables measuring the impedance of the bio-potential electrodes.

The ASIC, fabricated in a 0.5μm CMOS process, measures 17.55mm^2 and consumes only 200μW. Such low power consumption enables it to operate for more than 1 month on a standard coin cell battery, such as a CR2032. This makes the chip ideal for use in autonomous appliances.

EEG signals are μV-range low-frequency signals that suffer from a large amount of common-mode interference. Furthermore, the bio-potential electrodes needed to sense the signals generate a non-negligible offset. To achieve signal extraction, the ASIC requires readout front-ends with high common-

Continued on page 8

PATENTS > 9 | AWARDS > 11 | EVENTS > 16

Editorial

Research groups and IC manufacturers are scrambling for a part of the 3D action. And the first appliances with 3D chips are already available, with many more to come. But there are also a lot of questions surrounding 3D. Will 3D be limited to niche applications or will it become a widespread technology, as common as 2D CMOS process technology today? What is the roadmap for 3D, and which of the many technical options will be used? Will 3D allow us to maintain the Moore momentum? Will 3D be cost-effective?

Commercial 3D chips are mainly packages of Flash memory chips used, for example, in USB sticks or solid-state disks. Essentially, what we do is take a number of 2D chips and wirebond them in one package. This is a packaging technology only. It is cost-driven, and it is well understood. But that does not mean there is no room for innovation. At IMEC, for example, we look into developing 3D-WLP stacks using wafer-level packaging (WLP) technologies such as redistribution, flip-chip bumping and through-silicon vias. In such stacks, we combine heterogeneous functions, such as logic, memory, and analog sensors.

But 3D promises to be more than stacking 2D chips by connecting bond pads from one die to the other. Tighter 3D integration will be necessary to keep doubling the density of designs every 2 years, in line with Moore's law. This requires splitting the IC design itself into multiple stacked physical layers, which we call 3D-stacked ICs or 3D-SIC. And eventually, we could think of stacking and connecting chips at the level of transistors, arriving at a 3D-IC.

Research and industry are already tackling the technical aspects of 3D-SIC/IC. One challenge is making small enough vias with high aspect ratios. Another one is handling wafers and chips thinned well below 50µm, at which level the chip may curl up, and show microcracks that influence the transistors' behavior. And when you finally have those ultra-thin chips with micrometer-sized vias, you have to find a way to position the vias of one chip precisely on the landing pads of the second chip, which is no trivial problem.

The really hard part of 3D-SIC/IC technology, however, will be the design. The use of dense through-silicon vias allows designs that solve some of the interconnection problems of 2D designs. But at the same time, the complexity of 3D is many times that of 2D, involving issues such as testability, yield, quality, heat management, signal integrity, and choice of approach.

IMEC is one of the only centers that combines research on advanced 3D technology and research on 3D design. IMEC's 3D industrial affiliation program (IIAP) targets 3D-WLP, 3D-SIC, and 3D design. It allows industry players to join our research efforts, sharing the costs, risks, talents, and IP of 3D research.

One task within the program is to demonstrate the process steps of 3D integration, and to measure and improve the reliability and yield of real silicon implementations of 3D modules. At the same time, we will draw up predictive design rules and models for the 3D technology community.

And to exploit all benefits of 3D technology, design and technology options should be optimized together. Therefore we are looking into path-finding methods, comparing the relative pros and cons of the many technology and design options.

Another issue is that 3D needs classification and roadmapping, as we learned from mainstream CMOS. The industry is currently looking at too many options and paths, and the tools and equipment suppliers can no longer see the wood for the 3D trees. For this reason, IMEC will organize a workshop in Taiwan, later this year. This meeting will bring major 3D players round the table to discuss 3D issues and options, and to agree on conventions and roadmaps.

Eric Beyne, IMEC Scientific Director for Interconnect Technologies

NEWS FLASH

A joint initiative to bring science and technology to life **through art and design**

Addictlab and IMEC are launching a new call for ideas and visions on future applications of emerging technologies in the field of art, design, architecture, fashion, communication, environments, health and well-being. After a first successful collaboration researching visual, conceptual and more practical ways of communicating about nanotechnology, a new call will take it one step further into the world of emerging technologies and their applications, with a focus on the emerging invisible (a-material) production, where benefits are perceptions centred. The Addict & IMEC partnership is also aimed at creating a brand new international platform for creative views on nanotechnology applications and ideas. An international jury will select a winner for each application domain and announce it during a public event in 2009.

It all started a year ago. IMEC is driven by a dream: opening up the horizon of emerging technologies research, not only by widening the fields of scientific studies, but involving and informing as many people as possible. Science is for all, not only an educational topic, but also as a mean of increasing creativity and creating a true dialogue on science, technology, possible applications and implications. By crossing the borders between science and technology and art and design industry, research institutes, academia and policy leaders can enter into a dialogue with the broad public.

In this aim, IMEC came to Ad!dict Creative Lab (www.addictlab.com) for a first project that resulted in a publication: #27 Nanotechnology. This Inspiration Book generated workshops and exhibitions during 2007, and it's still adopted at IMEC as a communication tool to explain that science and creativity have no limits. The present project needs to be considered as a step further: emerging technologies are becoming privileged media in art and design. Even if still delimited to a niche category (e.g. bio-art, interactive or experience design, etc.) we all know that in an optic of sustainable development, this might be the future. The Addict Inspiration Book #29 'in.tangible.scape.s' will go through that entire invisible domain that is moving the creativity world from the object predominance to the experiencing sphere of perceptions and the benefits of a more and more invisible (a-material) production. This call reaches out to designers, artists, students, architects, engineers, researchers and dreamers worldwide. This second step will lead Addict with its labmembers and IMEC to the promotion of a new global approach of science and high-tech applied to arts and design in the wider sense.

Index

EDITORIAL	2
TECHNOLOGY REPORTS	
New ISM-band ranging transceiver allows positioning in decimeter range	5
Integrated analog front-end for broadband communication over power lines	6
IMEC reports progress on lithography at SPIE conference	6
IMEC in fast-forward towards optimized TANOS Flash technology	7
Plasma texturing and porous Si mirrors boost thin-film Si solar cell efficiency	8
Wireless sensor platform with integrated accelerometer	11
Hydrogen sensor with record ultra-low-power consumption	12
Software for automatic dialogue replacement in the post-production of motion pictures	14
NEWSFLASHES	
IMEC reports three ADC converters with record power efficiency	1
IMEC presents acquisition chip for ambulatory EEG systems	1
A joint initiative to bring science and technology to life through art and design	3
Methodology to analyze process variability compatible with DFM tools	4
With CleanC, IMEC sets a first step towards standardizing C code for multiprocessor system-on-chip	5
IMEC obtains record conversion efficiency of 24.7% for GaAs solar cells on Ge substrate	9
Wireless EEG system self-powered by body heat and light	10
Breakthrough organic RFID tag	12
INDUSTRY LINK	
Powerchip partners with IMEC on sub-32nm CMOS research	7
AMI Semiconductor and IMEC collaborate for next-generation Smart Power Technologies	7
EUROPEAN PROJECTS	
Europractice IC Service expands to MEMS Prototyping	13
DUALLOGIC to break the performance barrier beyond 22nm CMOS technology	13
PATENTS	9
AWARDS	11
COURSES	15
COLOPHON	15
EVENTS	16

NEWS FLASH

Methodology to analyze **process variability compatible with DFM tools**

At the 2008 Design, Automation & Test (DATE) conference, IMEC presented a variability-aware modeling (VAM) flow that analyzes process variability of sub-45nm technology. VAM enables designers to optimize their system design for timing, energy and yield at an expected load. It assesses the impact of process variation and degradation effects on the system performance, enabling predictive assessments of designs. IMEC's VAM flow can hook into commercial design for manufacturing (DFM) tools and has been validated on data from industrial process technology and on IP cores.

IMEC developed the VAM flow leveraging on its expertise in advanced sub-45nm process technology and system design technology. The VAM flow percolates information on process variability of sub-45nm technology from the transistor up to the system level. It enables IP block and system designers to assess and predict architecture design options and to identify design bottlenecks before manufacturing. This allows overcoming functional problems and parametric uncertainty of designs caused by process and material variability of deep sub-micron technologies. IMEC validated the VAM flow on commercial TSMC 45nm variability data, estimating the performance and energy needs for an ARM926 processor. The VAM output was used to optimize the processor before manufacturing using a commercial tool flow.

IMEC invites IDMs, fabless system companies, fabless digital IP providers and foundries to collaborate in its Technology-Aware Design (TAD) program. The program aims to develop the tools needed to design reliable systems with variable and unreliable components. Up to now, most variability characterization work is done internally at IDMs on their own technology and IP blocks. However, with the move to fabless and fablite companies, IMEC wants to bridge the gap between foundry and fabless companies on the design-level impact of using advanced semiconductor technologies. IMEC's TAD program is compatible with the confidentiality constraints for high-value proprietary IP blocks.

Qualcomm and Samsung are the 2 first top-tier industrial partners in IMEC's Technology-Aware Design program. IMEC has recently also signed a cooperation agreement with SI2 to pursue alignment with industry standardization efforts for SSTA.

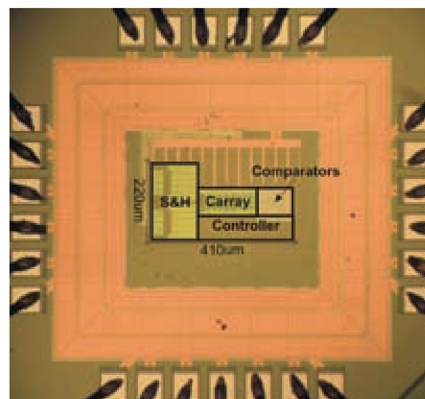
Continued from p.1

IMEC reports three ADC converters with record power efficiency

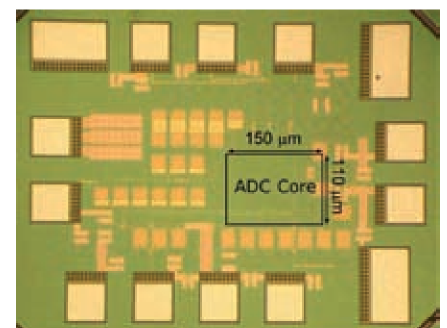
Further improving its own record SAR ADC, IMEC stepped up the power efficiency and made its ADC noise-robust.
IMEC realized a 9bit 40MSamples/s fully-dynamic noise-tolerant successive approximation (SAR) ADC achieving a record figure of merit of 54fJ/conversion step. This is a 16% improvement compared to last year's record design presented at ISSCC. That ADC was the world's first charged-based SAR ADC using charge-domain signal processing to overcome the fundamental power bottlenecks in successive approximation ADCs. The new design is optimized with an improved sample-and-hold and a noise-robust approach by leveraging redundancy in the search algorithm. The ADC was fabricated in 90nm digital CMOS and occupies less than 220x410µm². Measurements on silicon show a differential non-linearity (DNL) and integral non-linearity (INL) of respectively 0.7/-0.45LSB and 0.56/-0.65LSB.

For Flash ADC with sampling speed above 500MSamples/s, IMEC improves the figure of merit by a factor of 3.
IMEC realized a 5bit 1.75Gsamples/s folding Flash ADC in 90nm digital CMOS with a record figure of merit of 50fJ per conversion step. This is 3 times better than the best ever reported converters with sampling speeds over 500Msamples/s. Flash ADCs are typically used for high-speed applications. In this design, the fundamental power and area limits of Flash ADCs are overcome by using a factor 2 folding technique with dynamic power consumption only and without using amplifiers. In this way, the number of comparators could be reduced from 31 to 16 for a 5bit resolution.

The folding Flash ADC was made in 90nm digital CMOS, and occupies less than 110x150µm². Measurements at 1.75GSamples/s with a least significant bit (LSB) size of 25mV show an INL and DNL between -0.28/+0.24LSB and -0.29/+0.26LSB respectively.



9bit 40Msamples/s noise-tolerant dynamic SAR ADC attaining 54fJ per conversion step.



5bit 1.75Gsamples/s folding Flash ADC with 50fJ per conversion step.

NEWS FLASH

With CleanC, IMEC sets a first step towards **standardizing C code for multiprocessor system-on-chip**

IMEC has introduced a new programming style for C code, called CleanC. CleanC substantially improves the parallelization potential for code that will run on multiprocessor systems. IMEC's plug-ins for CleanC compliance analysis are freely available (www.imec.be/cleanc).

IMEC develops design tools for multiprocessor system-on-chip (MPSoC) that efficiently distribute applications over multiple processors, taking care of synchronizing tasks and exchanging data between tasks. These design tools analyze the source code of the applications, typically written in ANSI-C. The best results are obtained when the code conforms to a number of restrictions. IMEC has bundled these and called the resulting programming style CleanC. CleanC is essentially ANSI-C code written in a way that it is multiprocessor-friendly.

To enable developers to write CleanC suitable for parallelization and mapping on multiprocessor platforms, IMEC is developing a code refactoring toolbox. First, the CleanC compliance plug-ins will analyze the application code and flag violations of the CleanC programming style. Second, code transformations controlled by the user make the code compliant with the CleanC programming style. IMEC is developing interactive refactoring tools to improve this code optimization.

IMEC offers its tools for CleanC compliance analysis to the industry free of charge. The tools are plug-ins for the Eclipse/CDT development environment for C and C++ applications. The interactive CleanC environment extracts and visualizes the function call graph, and detects code fragments that are potentially hard to analyze by the MPSoC design tools and would lead to suboptimal solutions.

TECHNOLOGY REPORT

New ISM-band ranging transceiver allows positioning in decimeter range

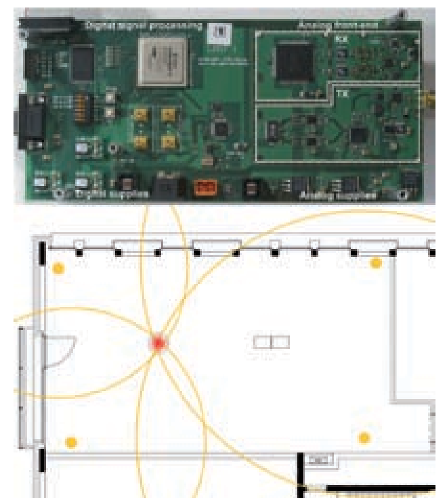
INTEC, IMEC's associated laboratory at Ghent University, and IMEC spin-off Essensium have successfully developed a demonstrator of an ISM-band ranging transceiver. The transceiver is based on a new concept that has been patented by Essensium. The location precision of the device is significantly better than that of existing technologies. The demonstrator is a proof-of-concept for further CMOS integration, and for many promising applications.

Most existing positioning technologies, such as GPS, address outdoor scenarios. These are satisfactory for outdoor use, especially when a clear enough line-of-sight is available. But they are no longer accurate when used indoor. This is mainly because of reflections and an obstructed line-of-sight, which complicates estimating the time-of-arrival of the broadcast signal.

Today's ISM-band ranging transceivers used in real-time local positioning claim an accuracy of 3 meter. However, actual tests show that an accuracy of 3 meter can often only be reached in the open. In other environments, with more obstacles, the accuracy will decline to 6 to 10 meter. More recently, UWB transceivers have been designed to reach decimeter accuracy. These, however, have a limited range because their maximum allowable output power is limited.
The concept of Essensium combines the best of both worlds, using wide band pulse techniques in the ISM band, and transmitting at significantly higher power. This translates in a good range precision over large distances with a single pulse. The demonstrator shows decimeter position accuracy even at distances well above 50 meter.

The starting point of this proof-of-concept was the patented idea of Essensium. Next, INTEC designed and built the hardware. This also included the 2.4GHz RF transceiver with the embedded location circuits. Essensium designed and implemented the digital signal processing and embedded control software needed for the high-accuracy ranging. The ISM-band ranging transceiver was developed using commercially available parts. The PCB design includes a 2.4GHz analog front-end, analog base band signal processing, a high-speed ADC, and nanosecond real-time embedded digital signal processing in FPGA. Next to showing decimeter positioning accuracy, the transceiver also proved to be resilient to interference with other data traffic in the same frequency band.

Continuing research targets low-cost and low-power integration into silicon of the ranging transceiver functions, with data communication in a single front-end. This research project is funded by the Flemish Institute for the Promotion of Innovation through Science and Technology (IWT) under contract 60393, ELOCA.



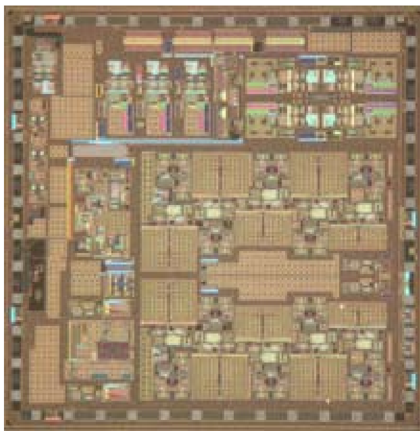
Essensium/INTEC ISM-band ranging transceiver.

Integrated analog front-end for broadband communication over power lines

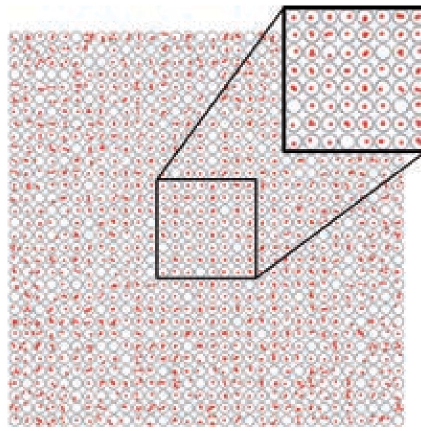
INTEC, IMEC's associated laboratory at Ghent University, has developed a power line front-end IC with unprecedented dynamic and tuning range, marking a significant improvement compared to existing devices.

Broadband over power lines (BPL) promises low-cost broadband communication over the existing power grid. The main advantage of BPL over other broadband technology is that no extra cables are needed. Every office, apartment, or house is connected to the power grid. But the BPL technology also faces technical challenges, mainly because power cabling is not designed to carry high-frequency signals.

Due to the increasing demand for bandwidth, the emerging standards specify tuning ranges well above the currently used 20 or 30MHz. And they make sharing the power lines with other power line systems through frequency division multiplexing mandatory. This requires analog front-ends with a very high dynamic range. And a high degree of integration will be needed to achieve low cost. INTEC's design (patent pending) offers a 60MHz tuning range, doubling the range of existing technologies. And it provides the highest dynamic range to date. The receiver operates linearly up to the breakdown voltage of the chip IOs and the noise floor (-144.5dBm/Hz) is more than 10dB below typical power line noise levels. Moreover, the architecture provides a high flexibility for frequency and bandwidth selection and integrates active filters, calibrated in the background, to eliminate interfering signals prior to AD conversion. High-density modulation schemes (e.g. 1024 QAM) and a high number of carriers (e.g. 1024) can be used, with an error vector magnitude below 1% rms.



The power line analog front-end chip.



1024 QAM for 40dB TX-RX attenuation.

The front-end IC, developed in STMicroelectronics 0.25µm SiGe BiCMOS technology, outperformed the major commercial power line transceivers in a field trial in Neuchâtel, Switzerland.

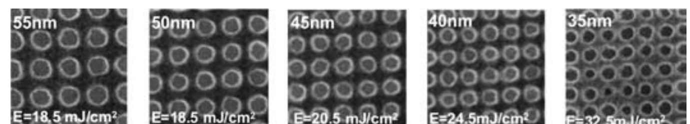
This project is funded by the European Commission (FP6 POWERNET). POWERNET also contributed to the sole MAC/PHY proposal remaining in the IEEE P1901 work group process, aiming at an international standard for inhome and access power line communication technology.

IMEC reports progress on **lithography** at SPIE conference

At the 2008 SPIE Advanced Lithography Conference, IMEC presented several papers that report on the state-of-the-art in lithography, and the issues that IMEC is working on. The papers cover both double patterning lithography and EUV lithography, 2 domains where most of the research efforts are concentrated on.

In one paper, co-authored by ASML, IMEC looks into the overlay and CD budgets – both for traditional litho-etch approaches, and for spacer-defined double patterning, comparing the pros and cons of both approaches. A second paper examines possible improvements of the cost-of-ownership of double patterning. IMEC looked at various resist processes currently developed by the resist companies to avoid the intermediate etch step in double patterning. The paper presents a few alternative resist processes that look promising for replacing the intermediate etch step. The third double patterning article focuses on overlay budgets. It examines various hard mask strategies for the double patterning process – especially focusing on process-induced overlay effects that come with these hard masks. For various hard mask approaches, IMEC has shown that the overlay needed for the 32nm technology node can be obtained on real product wafers. As for IMEC's EUV papers presented at the conference, a first one summarizes IMEC's imaging results obtained with ASML's EUV alpha demo tool. For now, IMEC has concentrated mainly on the contact hole level. This is the most critical level for optical litho to cover, and it is where EUV can be most helpful now. IMEC also showed the first results of a 32nm SRAM cell it has developed, and in which the contact hole level is exposed by EUV lithography. In a second EUV paper, IMEC covers the mask infrastructure for EUV reticles, looking at the imaging performance of masks that are manufactured at various mask shops (merchant and captive). The paper also points to some trends for the future, indicating how the mask absorber thickness can be reduced to drive EUV to smaller dimensions.

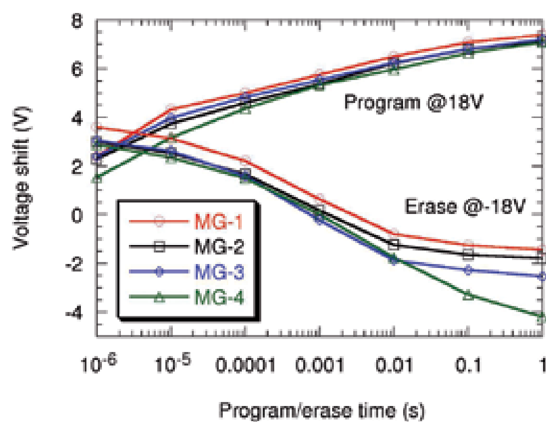
Resolution of contact holes down to 35nm, exposed with EUV at best focus.



IMEC in *fast-forward* towards **optimized TANOS Flash technology**

IMEC has fabricated a TANOS-type Flash memory cell based on an optimized stack of nitride and Al_2O_3 layers and a Ta-based metal gate. The TANOS stack shows excellent program and erase functionality, while maintaining good retention.

When approaching inter-memory cell geometries in the order of 30nm, electrostatic interference starts limiting the signal integrity, especially in the case of multilevel programming. This technique, which is now common practice in state-of-the-art Flash chips, allows programming two bits in one cell, reducing the bit size by one generation for the same layout rule. However, because of the smaller margins between the programmed levels, it is mandatory to reduce the impact of electrostatics. If this issue is not tackled, the data content of the memory will no longer be sharply defined. The most straightforward way of doing this is replacing the floating gate by a local charge trapping layer, typically a nitride layer (in TANOS, N stands for nitride). To obtain sufficient window, a high-k top layer (A stands for Al_2O_3) is needed, as well as a metal gate (T stands for Ta-based metal gate).



Program/erase transient of TANOS stacks with different metal gates. Selecting the right metal gate allows to open up the window substantially on the erased side without giving in on the programmed side.

IMEC's Flash program devotes a lot of effort into optimizing a TANOS cell as an alternative for the standard floating gate cell in NAND Flash technology. In recent experiments, IMEC has been comparing different nitride layers, different Al_2O_3 layers as well as different Ta-based metal gates in a joint development project with Applied Materials. The result was the identification of a so-called best known solution (BKS). This winner stack allows to open up the window substantially on the erased side (in this way creating additional margin for the multilevel scheme) while maintaining good retention and cycling endurance, which is a substantial breakthrough with respect to previous results. In the broader scope of its Flash memory program, in cooperation with major Flash memory manufacturers, IMEC continues to work with different suppliers to further optimize the stack.

The resulting device is a major milestone towards the replacement of floating gate NAND by TANOS technology for the 30nm generations and below.

Powerchip partners with IMEC on **sub-32nm CMOS research**

Powerchip Semiconductor Corporation (PSC), a leading Taiwan-based memory semiconductor supplier offering DRAM and Flash memory chips, partners with IMEC to do R&D for the sub-32nm memory process generations.

As part of the agreement, PSC will collaborate within IMEC's advanced lithography program, addressing immersion, double patterning and EUV lithography. Since March 2008, PSC researchers work at IMEC, closely collaborating with IMEC's researchers.

With this agreement, IMEC further strengthens its consortium and program on leading memory technologies.

AMI Semiconductor and IMEC collaborate for **next-generation Smart Power Technologies**

AMI Semiconductor (AMIS), recently acquired by ON Semiconductor, started a new two-year collaboration program with IMEC to develop the next generation of Smart Power Technologies. AMIS is a leading designer and manufacturer of state-of-the-art mixed-signal and digital products for the automotive, medical, industrial, aerospace, and high-voltage communication markets.

AMIS will develop critical and novel Smart Power processes and devices in IMEC's 200mm facilities, using IMEC's know-how and experience in deep sub-micron process technology. A team of AMIS engineers will join the IMEC engineers in Leuven. They will work in close collaboration with the AMIS Smart Power team in Oudenaarde, Belgium.

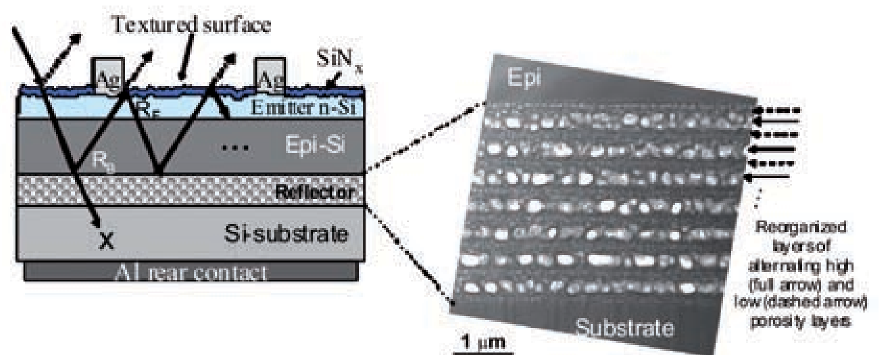
Plasma texturing and porous Si mirrors **boost thin-film Si solar cell efficiency**

IMEC's thin-film Si solar cells on low-cost substrates have reached efficiencies close to 14%. This record value was obtained by implementing an optimized front surface texture and by incorporating an intermediate reflector at the epi/substrate interface.

Thin-film Si solar cells, consisting of an epitaxially grown active layer on a low-quality highly doped Si substrate, incorporate many attractive features usually associated with their sister cells based on bulk Si. Although they have a very similar production process, thin-film Si solar cells offer a cheaper alternative, since only a very thin (20μm or less) active layer of the expensive high-quality crystalline Si is required. However, the efficiency of epitaxial semi-industrial screen-printed cells today is limited to only 11-12%. For this reason, the PV industry currently has little interest in this type of solar cell. One of the main reasons for the low efficiency of these cells is that light traversing the epitaxial layer is absorbed in the low-quality substrate and is therefore lost for collection, resulting in a low short-circuit current (J_{sc}). IMEC has now tackled this problem by improving the optical path length for long-wavelength light in a twofold way.

Firstly, fluorine-based plasma texturing of thin-film crystalline Si solar cells has allowed reducing the front surface reflectance to values below 20% (before antireflection coating). The Si removal could be limited to 1-2μm, ensuring an effective scattering of light, as shown by the analysis of angular resolved reflection measurements. In case of a prolonged texturing, the effective path length is enhanced by a factor of two.

Secondly, an intermediate reflector has been positioned at the epi/substrate interface to enhance the absorption volume in the epitaxial layer. Photons reaching this interface can now be reflected either by positive interference or by total internal reflectance (TIR). As a result, a second or even multiple passes through the epitaxial layer become possible. In practice, the reflector consists of a porous Si stack containing alternating high- and low-porosity layers (a multiple Bragg reflector), which is formed by electrochemical anodization. Due to both the Bragg effect and TIR, this stack acts as an effective internal reflector. An internal reflection of 80% and a short-circuit current increase of 3mA/cm^2 have been achieved when incorporating a 15-layer porous Si stack. This corresponds to a path length enhancement of 7. Results can even be improved by using an optimized reflector design, based on 'chirping' the reflector structure. In such a design, the thicknesses of the low- and high-porosity sublayers vary with the depth, which can lead to a substantial bandwidth enlargement of the reflector. With these specialized structures, a record efficiency of 13.9% and J_{sc} of 29.6mA/cm^2 was reached with an industrial type cell process based on screen-printed metallization on a low-cost Si substrate.



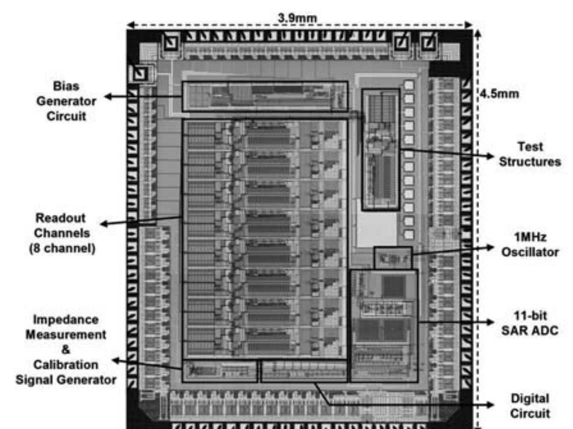
(Left) advanced epitaxial cell layout illustrating the concept of an intermediate reflector. (Right) transmission electron microscopy picture of a reorganized porous Si stack.

Continued from p.1

IMEC presents acquisition chip for ambulatory EEG systems

mode rejection ratio (CMRR), low-noise, and high-pass filter characteristics to filter the differential electrode offset voltage. The implemented front-end is based on AC-coupled chopper-stabilized instrumentation amplifiers with a DC-servo loop outside the choppers for the high-pass filtering. Each channel has adjustable high-pass filtering (cut-off at 0.1Hz) and the gain and bandwidth can be selected electronically. The front-ends achieve the lowest noise-efficiency factor (4.1) and the highest CMRR (>120dB) ever reported. The large input impedance (>1G) ensures high CMRR even if there is a mismatch between the electrode impedances. Meeting the critical International Federation of Clinical Neurophysiology (IFCN) requirements makes this ASIC ready for clinical EEG systems.

The EEG ASIC can be used for miniaturized ambulatory EEG acquisition systems, increasing the patients' autonomy and quality of life. It's also suited for sports and entertainment appliances, comfort monitoring, and other health and lifestyle products and services. Interested parties can license the ASIC for further product development.



Die micrograph of IMEC's 8-channel EEG acquisition ASIC.

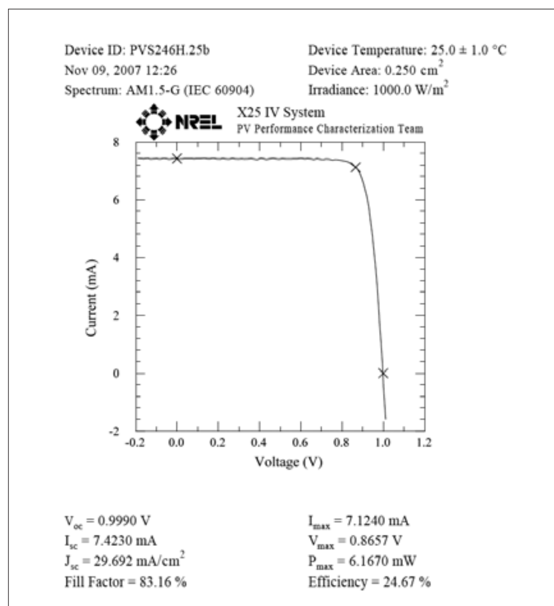
NEWS FLASH

IMEC obtains record conversion efficiency of **24.7% for GaAs solar cells on Ge substrate**

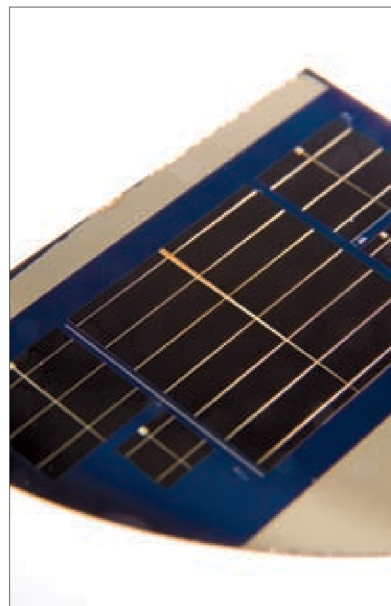
IMEC has realized a single-junction GaAs solar cell on a Ge substrate with a record conversion efficiency of 24.7%. The efficiency was measured and confirmed by NREL (National Renewable Energy Laboratory, US). GaAs solar cells are used in satellite solar panels and earth-based solar concentrators.

IMEC realized this record on a single-junction GaAs cell, grown epitaxially on a Ge substrate with an improved micro-defect distribution. The record cell measures 0.25cm^2, and shows an efficiency of 24.7%, with an open-circuit voltage (V_{oc}) of 999mV, a short-circuit current (J_{sc}) of 29.7mA/cm^2, and a fill factor of 83.2%. The cell was made under the ESA-IMAGER project. Umicore, a leading materials technology group, produced the Ge substrate through an optimized manufacturing technology, aimed at improving the intrinsic Ge crystal quality.

Improving the efficiency of this single-junction GaAs cell is a further step in the development of a hybrid monolithic/mechanically stacked triple-junction solar cell. This type of cells consists of stacks of solar cells made of different semiconductors, carefully chosen to absorb the solar spectrum as efficiently as possible. Among the many possible combinations, IMEC focuses on stacked cells consisting of top cells with III-V materials and bottom cells made from Ge. With this combination, IMEC is targeting a conversion efficiency of 35% and more. The resulting stacks can be used in satellites and earth-based concentrators, where high-efficiency energy conversion is paramount.



Performance characterization of IMEC's GaAs cell, as measured by NREL.



IMEC's single-junction GaAs solar cell on Ge substrate.

Patents

Europe

- *A method and apparatus for interleaving, deinterleaving. (EP 1 267 511)*
- *Method and apparatus for local surface analysis. (EP 1 318 394)*
- *Diffraction grating based fibre-to-waveguide coupler for polarisation independent photonic integrated circuits. (EP 1 353 200)*
- *Apparatus and methods for simultaneous surface acoustic wave and surface plasmon resonance measurements. (EP 1 636 560)*
- *Conjugated polymers provided with at least one MIP and a method for their preparation via conjugated macro-iniferters. (EP 1 647 560)*
- *Virtual NOC. (EP 1 744 497)*
- *Slot coupled micromachined waveguide antenna. (EP 1 052 726)*
- *A cross connect device and a method for switching based on space switching and grouping of channels. (EP 1 030 481)*

Japan

- *Method for bottomless deposition of barrier layers in integrated circuit metallization schemes. (JP 4043785)*
- *Solar cell and process of realisation thereof. (JP 4073968)*

Taiwan

- *SiGe strain relaxed buffer for high mobility devices and a method of fabricating it. (TW I287254)*
- *Method to enhance the initiation of film growth. (TW I289330)*

USA

- *Method and system for estimating and compensation IQ imbalance. (US 7,313,303)*
- *Method of fabrication of an infrared radiation detector and infrared detector device. (US 7,320,896)*
- *Semiconductor device fabricated by a method of reducing the contact resistance of the connection regions. (US 7,320,939)*
- *Method for depositing a group III-nitride material on a silicon substrate and device therefore. (US 7,327,036)*
- *Formation of deep via airgaps for three dimensional wafer to wafer interconnect. (US 7,338,896)*

NEWS FLASH

Wireless EEG system **self-powered** by body heat and light

In the framework of Holst Centre, IMEC has developed a battery-free wireless 2-channel EEG (electroencephalography or monitoring of brain waves) system powered by a hybrid power supply using body heat and ambient light. The hybrid power supply combines a thermoelectric generator that uses the heat dissipated from a person's temples and Si photovoltaic cells. The entire system is wearable and integrated into a device resembling headphones. The system can provide more than 1mW on average indoor, which is more than enough for the targeted application.

Thermoelectric generators using body heat typically show a drop in generated power when the ambient temperature is in range of the body temperature. Especially outside, the photovoltaic cells in the hybrid system counter this energy drop and ensure a continuous power generation. Moreover, they serve as part of the radiators for the thermoelectric generator, which are required to obtain high efficiency.

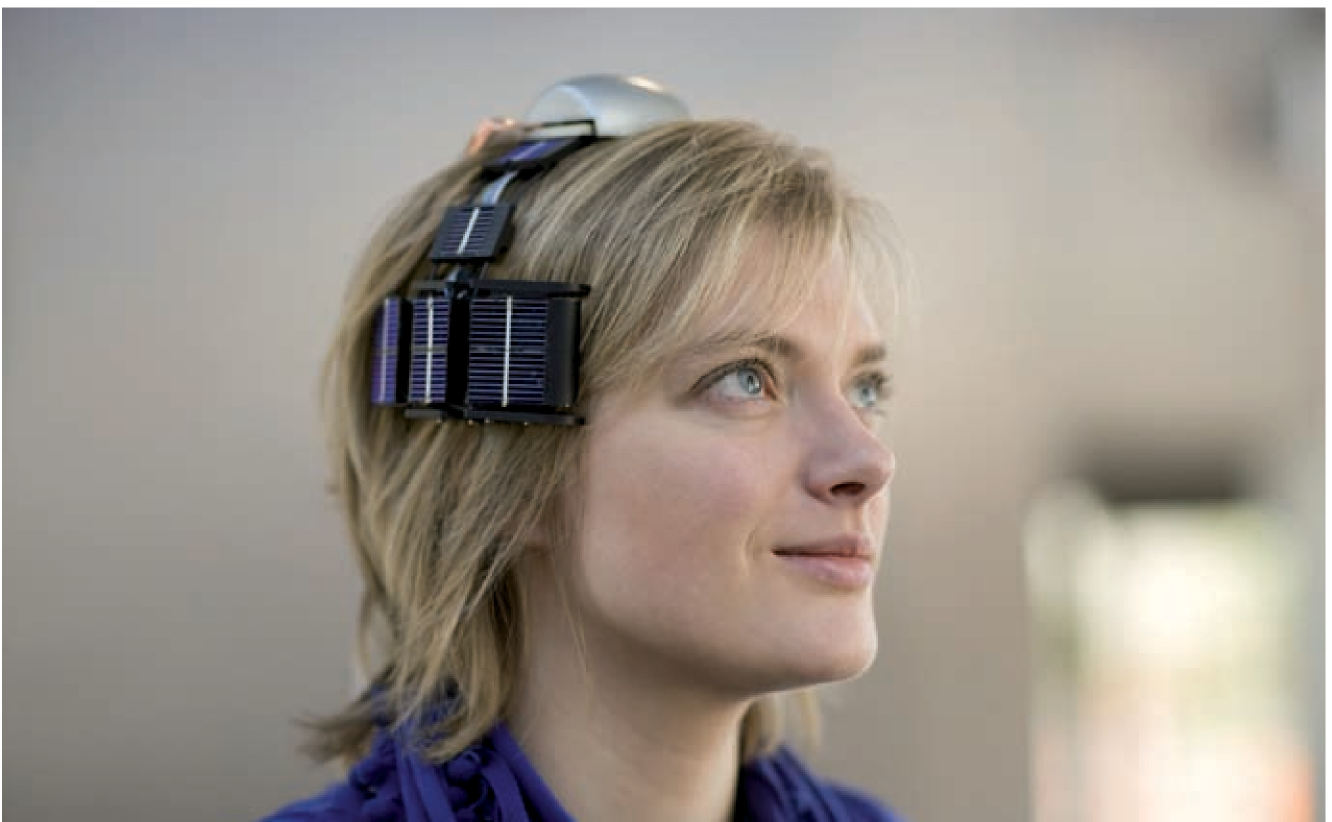
Compared to a previous EEG demonstrator developed within Holst Centre, which was solely powered by thermoelectric generators positioned on the forehead, the hybrid system has a reduced size and weight. Combined with full autonomous operation, no maintenance and an acceptable low heat flow from the head, it further increases the patient's autonomy and quality of life. Potential applications are detection of imbalance between the two halves of the brain, detection of certain kinds of brain trauma and monitoring of brain activity.

The system is a tangible demonstrator of Holst Centre's Human++ program researching healthcare, lifestyle and sport applications of body area networks. Future research targets further reduction of the power consumption of the different system components of the body area network as well as a significant reduction of the production cost by using micromachining. Interested parties can get more insight in this research or license the underlying technologies through membership of the program.

Technical details

The thermoelectric generator is composed of six thermoelectric units made up from miniature commercial thermopiles. Each of the two radiators, on left and right sides of the head, has an external area of 4x8cm^2 that is made of high-efficiency Si photovoltaic cells. Further, thermally conductive comb-type structures (so-called thermal shunts) have been used to eliminate the thermal barrier between the skin and the thermopiles that is caused by the person's hair on the thermoelectric generator.

The EEG system uses IMEC's proprietary ultra-low-power biopotential readout application-specific integrated circuit (ASIC) to extract high-quality EEG signals with micro-power consumption. A low-power digital-signal processing block encodes the extracted EEG data, which are sent to a PC via a 2.4GHz wireless radio link. The whole system consumes only 0.8mW, well below the power produced to provide full autonomy.



The wearable wireless EEG system with hybrid power supply.

The R&D for the Wireless Autonomous Transducer Solutions program (WATS) is carried out by IMEC's sister company IMEC–NL at Holst Centre.

Wireless sensor platform with **integrated accelerometer**

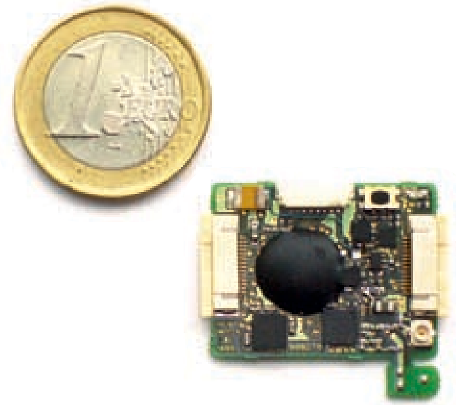
In the framework of Holst Centre, IMEC has developed a new wireless sensor platform. The new sensor has a battery, radio, microprocessor and accelerometer. And it comes with a host of connecting possibilities, making it suitable for use with power scavengers, readout chips, sensor networks, etc. It will be used at the heart of new sensing applications for the body area network (BAN) in the Human++ program.

The new platform consists of a Texas Instruments ultra-low-power MSP430F1611 microcontroller and a Nordic nRF24L01 radio chip. The accelerometer is either an ADXL320 3D 2g accelerometer or an ADXL321 2D 18g accelerometer. The 2g accelerometer will be used in BAN applications, including sensing and measuring human body movements. The sensor with the 18g accelerometer is more suited for industrial applications, measuring for example vibrations in cars.

The sensing platform can be easily integrated and modified; it has many possibilities to connect to other devices. For example, two flexible flat cable (FFC) connectors allow adding alternative sensors. And depending on the application, the platform can be wired to an antenna-on-chip, an external antenna with micro-coaxial connector, or a wire antenna. The platform may also be connected to energy scavengers, bypassing the battery circuit.

The system is started through a micro push button. After it is switched on, the push button takes whatever function that is programmed in the application. It can for example be used to select a different working modus. Also programmable is the way the platform is shut down. A shutdown is possible, for example, when the battery runs low, when the base station sends a shutdown command, or when the base station is out of reach for a certain time. And when the platform is down, the power leakage is only a fraction of the battery self discharge.

The power consumption of the platform strongly depends on the application that it is running. The maximum power consumption is 28mA when the application is continually in receive mode. Future applications are targeted to consume less than 1mA. And in shutdown, the platform uses less than 1nA.



Wireless sensor platform.

SPECIFICATIONS:
- 20.5mm x 25mm
- MSP430F1611 TI ultra-low-power microcontroller
- nRF24L01 Nordic low-power 2.4GHz 2mbps radio transceiver
- ADXL330 3D 2g accelerometer or ADXL321 2D 18g accelerometer
- 160mAh Lithium-Ion battery
- Dual-function soft power-on push button
- Chip antenna, wire or external antenna

CONNECTIONS:
- Antenna
- JTAG interface
- 12x digital I/O
- 1x SPI or UART
- 8x 12bit ADC (3 used for accelerometer)
- 2x 12bit DAC
- 2x timer functions
- V_{cc}
- V_{batt}
- ADC V_{ref}

Awards

- Stefan Pauwen has received the **Alcatel-Lucent 2007 Best Thesis Award** for his work entitled 'RF-power actuation of RF-MEMS', realized under daily advisory at IMEC from X. Rottenberg, K. Vaesen and W. De Raedt and at KULeuven from Prof. Nauwelaers and Prof. Mertens.
- The article 'Pulse oximeter fully powered by human body heat' from T. Torfs, V. Leonov, IMEC; and R. Vullers, IMEC-NL/Holst Centre has been chosen as the **best article published in Sensors & Transducers Journal** (ISSN 1726-5479) **in 2007**. The criteria were: novelty, innovation, outstanding new research and current importance.
- Frederic Dross has received the **Young Researcher Award** at the 17th International Photovoltaic Science and Engineering Conference (2007) for his paper entitled 'A new method for the production of ultra-thin crystalline Si wafers'. Authors of the paper are: F. Dross, A. Milhe (also at Ecole des Mines de Paris (CEMEF), France), J. Robbelein, I. Gordon, P.O. Bouchard (CEMEF), G. Beaucarne and J. Poortmans.
- On his website, 'lithoguru' Chris Mack nominated the paper of Lieve Van Look as the **best paper** (out of 700) **of the SPIE 2008 Conference**. The paper is entitled 'Tool-to-tool optical proximity effect matching'. Authors are L. Van Look, J. Bekaert, P. De Bisschop, J. Van de Kerkhove, G. Vandenberghe, IMEC; K. Schreel, J. Menger, G. Schiffelers, E. Knols, R. Willekers, ASML (The Netherlands).
- Frederik Van Laere (INTEC, IMEC's associated laboratory at Ghent University) has received the **Corning Outstanding Student Paper Award** at the Optical Fiber Communication Conference 2008, for his paper entitled 'Multifunctional photonic crystal compact demux-detector on InP'. Authors are F. Van Laere, T. Stomeo, M. Ayre, C. Cambournac, H. Benisty, T.F. Krauss, D. Van Thourhout and R. Baets.
- The paper entitled 'Backside thinned CMOS imagers with high broadband quantum efficiency using a new integration process', published in Electronics Letters, Vol. 44, n°1, January 2008, has been selected as **Letter of the Month**. Authors of the paper are K. De Munck, J. Bogaerts, D.S. Tezcan, P. De Moor, S. Sedky (American University in Cairo, Egypt) and C. Van Hoof.
- Wilfried Vandervorst will be **keynote speaker** at the 2008 Nanoscale VI Conference's session on 'beyond topography – measurement of physical properties at the nanoscale'.
- Cor Claeys has been elected as **President of the IEEE Electron Devices Society** (EDS) for 2008-2009.

NEWS FLASH

Breakthrough **organic RFID tag**

At the 2008 International Solid State Circuit Conference (ISSCC), Holst Centre presented a plastic 64-bit inductively-coupled passive RFID tag operating at 13.56MHz. The tag is based on IMEC's plastic rectifier technology and Polymer Vision's organic electronics technology. With a record 780bit/s data readout of 64 bits over 10cm, the RFID tag approaches the requirements for item-level tagging. It generates bit rates that are 5 times higher than state-of-the-art plastic RFID systems, paving the way for low-cost RFID tags to replace barcodes.

The new RFID tag consists of a low-cost inductive antenna, a capacitor, plastic rectifier and plastic circuit, all on foil. The LC antenna resonates at 13.56MHz and powers up the organic rectifier with an AC voltage. From this voltage, the rectifier generates the 14V DC supply voltage for the 64-bit organic transponder chip, which drives the modulation transistor between the on and off state with a 64bit code sequence.

The breakthrough rectifier on foil is based on IMEC's rectifier technology. Organic vertical diodes have been used in the rectifier because they outperform organic transistors for rectification at frequencies at and above 13.56MHz. At an RF magnetic field strength of 1.26A/m, the rectifier generates an internal transponder supply voltage of 14V. At this voltage, the 64-bit code is read out at a data rate of 787bits/s. The reading distance is up to 10cm.

The organic 64bit transponder chip, made by Polymer Vision, uses organic bottom-gate p-type pentacene thin-film transistors from soluble precursor route. It has close to 400 transistors and is thus significantly smaller than previous designs.

The organic RFID was made within the framework of the Holst Centre research program on organic circuitry. Part of it was co-funded by the European project POLYAPPLY.

A fully flexible, 64-bit organic RFID tag generated by laminating the antenna foil, the organic rectifier foil and the 64-bit organic digital logic foil.

Hydrogen sensor with **record ultra-low-power consumption**

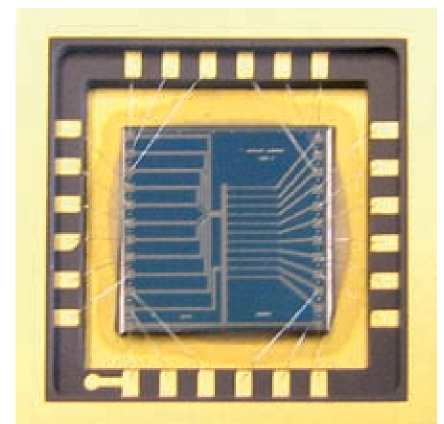
In the framework of Holst Centre, IMEC and Nanosens have developed an ultra-low-power hydrogen sensor based on palladium nanowires. It shows a reproducible response to hydrogen concentrations as low as 2.7ppm, while consuming a mere 1nW power. Sensors such as these can be used, for example, in fuel cells or to monitor for gas leaks.

Palladium is known as one of the best materials for hydrogen sensing, as it is able to absorb up to 600 times its own volume of hydrogen. In the presence of hydrogen, palladium forms the more resistive palladium-hydride. Such resistive sensor elements are of particular interest as they enable relatively straightforward signal detection and fabrication. For the palladium-based sensors that are currently available, the response times and sensitivity are insufficient; but more importantly, these sensors do not meet the ultra-low-power requirements for integration with wireless autonomous sensor nodes needed in many applications.

Nanosens, a Dutch company developing innovative nanotech solutions, has invented CMOS compatible processes to fabricate highly uniform, long, and small nanowires of various materials, including palladium.

At Holst Centre, chips with palladium nanowires have been subjected to a wide range of hydrogen concentrations in nitrogen. The sensor shows a reversible response to hydrogen concentrations as low as 2.7ppm while consuming a mere 1nW of power. To the best of our knowledge this is the hydrogen sensor with the lowest power consumption to date. Additionally, the sensor response to hydrogen is highly reproducible and stable over a period of up to six months. In a next step, a low-power read-out circuitry will be developed at Holst Centre. This will result in a full sensing device.

Hydrogen is widely used in many industries. It is also touted to become one of the main energy carriers of the future, replacing fossil fuels. Hydrogen sensors thus represent an important opportunity. They could be used in applications as varied as detecting impending electrical power transformer failure, or monitoring hydrogen concentrations in fuel cells. And for all hydrogen-based industrial applications, the availability of sensitive and effective hydrogen sensors to quickly respond to hydrogen gas leaks and to monitor manufacturing and distribution is paramount.



Hydrogen sensing chip.

Europractice IC Service expands to **MEMS prototyping**

IMEC, representing Europractice IC Service, and Tronics Microsystems SA collaborate to enable Europractice IC Service to add MEMS to its Multi-Project Wafer (MPW) programs. Tronics, a leading global manufacturer of custom MEMS components for demanding applications, is the first technology provider selected by IMEC to support Europractice IC Service's extension of its production portfolio to MEMS. It will give the program access to one of its MEMS on SOI technologies through regular MPW runs.

Since 1995, Europractice IC Service has brought ASIC design and manufacturing capability within the technical and financial reach of any university, research institute and company. Coordinated by IMEC, it offers low-cost ASIC prototyping and ASIC small-volume production through MPW and dedicated wafer runs at leading foundries and IC manufacturers, including AMI Semiconductor, austriamicrosystems, IHP, TSMC and UMC.

As a recognized leader and pioneer in SOI MEMS technologies, Tronics was the first MEMS manufacturer to offer a qualified industrial SOI-MEMS technology in an MPW service. The French manufacturer first offered a 20µm-thick SOI technology on MPW in 1999. The company upgraded its capabilities to 60µm-thick SOI High Aspect Ratio Micromachining with hermetic wafer-level packaging in 2006. This technology was originally introduced for the production of high performance accelerometers and gyroscopes. The process enables the creation of capacitive sensors, electrostatic actuators, resonators, energy scavengers and other innovative mechanical structures.

DUALLOGIC to break **the performance barrier beyond 22nm CMOS technology**

European research teams will investigate if high-mobility, non-Si channel materials could impact the CMOS generation beyond 22nm.

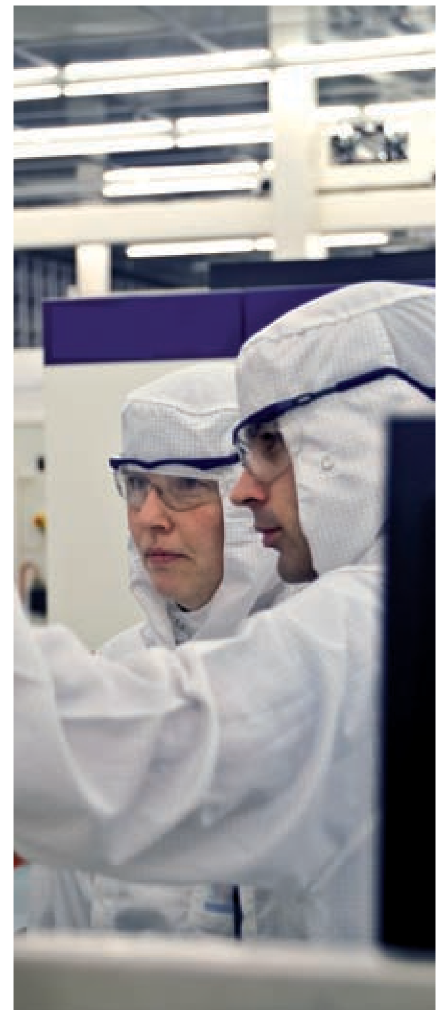
A large initiative has been launched in Europe with the kick-off of the project DUALLOGIC (dual-channel CMOS for (sub-)22nm high-performance logic), co-funded by the European Commission's 7th Framework program (FP7) in Information and Communication Technologies. DUALLOGIC aims to shape the CMOS generations beyond 22nm with breakthrough innovations in nano-electronic materials, equipment, processing and device integration on Si.

In DUALLOGIC, the research teams will attempt the co-integration of Ge pMOS and III-V nMOS side-by-side on a complex engineered substrate on Si to demonstrate for the first time a dual-channel CMOS technology. A European consortium consisting of NCSR DEMOKRITOS, IMEC, IBM-Zurich, CEA-LETI, STMicroelectronics, NXP Semiconductors, AIXTRON, University of Glasgow and Katholieke Universiteit Leuven, and with an EC grant of 5.8 million euro, is gathered for 36 months to tackle this challenging goal.

The main output of the project will be to demonstrate that a high-mobility dual-channel front-end-of-line (FEOL) CMOS technology is scalable and manufacturable by employing a Si-compatible process in a 65nm/200mm pilot line. Besides, the channel materials under investigation in this project have several other interesting properties which make them attractive beyond the context of device scaling for logic as, for example, in applications where lower supply voltages are needed to combine low power with high performance. Because of this, DUALLOGIC could create a generic material and technology platform which could allow a significant diversification on the chip with added functionality. Also, it could be the catalyst for the convergence of 2020 nanoelectronic technologies as foreseen in the ambitious research agenda of Europe's ENIAC technology platform.

DUALLOGIC will benefit a lot from IMEC's EXPLORE program on Ge and III-V. In the framework of the EXPLORE internal program, IMEC has already made significant advances in Ge pMOSFET downscaling through the development of halo implants, activation anneals, passivation and germanide contacts for source and drain. Moreover, IMEC is developing all in-situ III/V channel materials and associated high-k gate stacks in its own Riber 200mm MBE cluster. IMEC will bring to DUALLOGIC all the know-how it has already acquired to define short channel Ge pMOSFETs on GeOI substrates as well to co-integrate Ge pMOS and III/V nMOS on dual-channel engineered substrates, thus producing a large added value for the project.

More information:
www.ims.demokritos.gr/DUALLOGIC



IMEC in Future Fab's editorial board

The revamped Future Fab International magazine goes digital. You can download the latest edition at www.future-fab.com

Gilbert Declerck, CEO, IMEC and Lode Lauwers, Director Strategic Program Partnerships, IMEC participate in Future Fab's editorial board, sharing their experience and industry outlook with the semiconductor community.

EE Times considers IMEC as one of the '35 *people, places & things that will shape the future'*

"The Interuniversity Microelectronics Center bases its success on a fine-grained, 'pick and mix' approach to collaboration with industry that lets companies join in where and when they want. … IMEC has now reached the point where it is driving the global visionary agenda in key areas such as CMOS, mobile terminals, immersion and extreme-ultraviolet lithography, and EDA. Its European locus has always valued specialization and outreach; that will pay dividends in an Asian-oriented electronics industry. IMEC started with an emphasis on bringing the brightest engineers from around the world to conduct research in Europe. Its 1,500 researchers now represent more than 50 countries. The work they do will help determine how CMOS is delivered in the future and how the industry moves beyond that technology." By Peter Clarke (EE Times)

Read more: www.eetimes.com

TECHNOLOGY REPORT

Software for automatic dialogue replacement in the post-production of motion pictures

ETRO, IMEC's associated laboratory at the VUB (Vrije Universiteit Brussel), has developed software for automatic dialogue replacement, a post-production process for picture soundtracks. The software allows automatically editing a studio soundtrack, measuring its timing relationship with the original reference soundtrack and compensating for the lip synchronization errors by time-scaling the studio soundtrack. The output is a synthesized signal precisely synchronized with the picture.

During the post-production of soundtracks, it is often necessary to replace the original actors' dialogues recorded live on the film set by re-recorded studio dialogues. This is because the original recordings are distorted by background noise. But such dialogue replacement introduces, among others, lip synchronization errors. And it is very expensive and time-consuming.

The ETRO software aligns the soundtracks in several steps. To deal with difficult alignment pairs which, for example, have breathing pauses, a pre-processing step first classifies the soundtracks into speech and non-speech segments. For noisy soundtracks, for example corrupted by street noise, this is done through spectral subtraction techniques in combination with noise tracking algorithms for non-stationary environments.

Next, the original and studio recordings are spectrally analyzed to capture short-time variations. These are then used to measure the relative timing differences between the corresponding phonemes in both recordings. This is a measure for the amount of stretching and compression needed to optimally align the studio soundtrack with the reference track. In a second step, the timing discrepancies are cancelled out by time-scaling the studio soundtrack according to the measured time differences. In the resulting time-scaled output, the timing of the significant features conforms to the timing of the corresponding features in the original track.

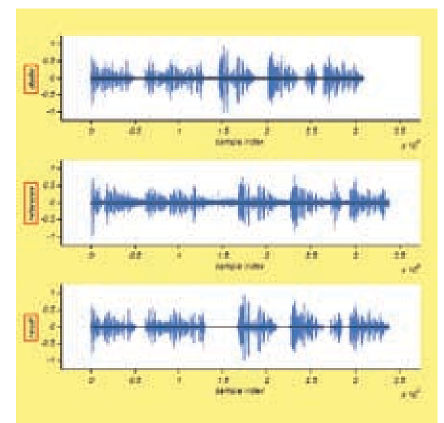
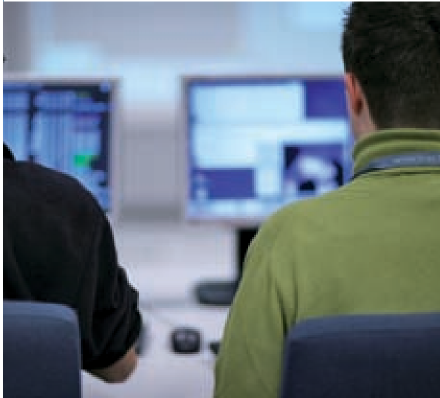


Illustration of the developed synchronization technique. Upper panel: studio recording which is not in sync with the video images; middle panel: audio that was originally recorded with the video and which is therefore lip-synchronized; lower panel: studio recording from the upper panel after automatic synchronization to the video reference (middle panel).

Demonstrations of the software are available at: http://www.etro.vub.ac.be/Research/DSSP/Projects/National/EOS_2007/demo_EOS.htm

MTC

MTC provides live webcasts of its courses and seminars



IMEC's Microelectronics Training Center MTC has a long-standing tradition of organizing training courses and seminars on a wide range of topics for IMEC employees, academics and industrial experts. To strengthen the international character of its training and seminar program, MTC now offers its industrial and academic partners the opportunity to attend courses or seminars broadcast life over the Internet. In addition, MTC already has a library of recorded seminars and training sessions that can be viewed on the Internet.

Live seminars and courses are available on request: mail to training@imec.be

Courses

- The following lectures are scheduled in the frame of the Capita Selecta on Nanoscience and Nanotechnology, a series of lectures that KULeuven and MTC organize on the latest developments in nanotechnology and related ethical questions:
  - Miniaturized bioanalytical sensors: challenges and opportunities
    May 6, 2008, KULeuven, Leuven, Belgium
  - The impact of military research on nanotechnology
    May 13, 2008, KULeuven, Leuven, Belgium
  - Nanostructures require characterization on the sub-nanometer scale
    May 20, 2008, IMEC, Leuven, Belgium

- **Plasma etching for CMOS technology and ULSI applications**
  May 13-15, 2008, IMEC, Leuven, Belgium
  The course provides an understanding of plasma processes for CMOS applications and ULSI technology. Fundamental and practical aspects of front-end and back-end plasma processes for deep sub-micron logic processes will be discussed.

- **SOI for analog, digital and RF SOCs and microsystems applications**
  May 15-16, 2008, IMEC, Leuven, Belgium
  This two-day training offers a broad perspective on the opportunities that silicon-on-insulator (SOI) opens in the field of low-voltage, low-power CMOS systems-on-chip, with an emphasis on analog and microwave functions, besides the widely demonstrated advantages of SOI for high-performance digital and memory applications.

- **Silicon processing for sub-90nm circuit fabrication**
  June 11-13, 2008, IMEC, Leuven, Belgium
  This course offers a comprehensive, state-of-the-art training program in the practice, fundamentals, and emerging trends of Si wafer processing focused on deep sub-micron devices.

- **Bottom-up and top-down nanotechnology**
  November 12-14, 2008, IMEC, Leuven, Belgium
  Organized by MTC and Marc Madou, University of California, Irvine, US
  Bottom-up and top-down nanotechnology is a course for the broad audience of scientists and engineers from industry and academia with a keen interest in which technologies will supersede current electronics. The course should help academic and industry decision makers to make educated decisions on future R&D investments.

More information and a full overview of courses: www.imec.be/mtc

COLOPHON

Publisher
Prof. Gilbert Declerck, CEO

Editors
Jan Provoost
Mieke Van Bavel

Director External Communications
Katrien Marent
IMEC vzw
Kapeldreef 75
B-3001 Leuven – Belgium
Phone: +32 16 281 880
Fax: +32 16 281 637
E-mail: Katrien.Marent@imec.be

USA contact
Raffaella Borzi
IMEC, Inc.
960 Saratoga Ave, Suite 206
CA 95129 – San Jose
California – USA
Phone: +1 408 551-4502
Fax: +1 408 551-4505
E-mail: Raffaella.Borzi@imec.be

China contact
Teng Gao
IMEC Shanghai Office
Units C60-C66, 11/F
Shanghai Mart
2299 Yan'an Road West
Shanghai 200336 – P.R. China
Phone: +86 21 6236-0700 ext. 18
Fax: +86 21 6236-0706
E-mail: Gao.Teng@imec.be

IMEC representative Japan
Akihiko Ishitani
IMEC Representative in Japan
c/o Rokubancho Kyodo Bldg. 1F - 6 Rokubancho
Chiyoda-ku - Tokyo 102-0085 - Japan
Phone: +81-3-5210-5882
Fax: +81-3-5210-5883
E-mail: Akihiko.Ishitani@imec.be

IMEC Taiwan
Prof. Tien-Fu Lei
A6, 1F, No.1, Li-Hsin 1st Rd.,
Hsinchu Science Park, Hsinchu, Taiwan
Phone: +886 3 5787828
E-mail: Tien-Fu.Lei@imec-tw.tw

Stichting IMEC Nederland
High Tech Campus 31
5656 AE Eindhoven
The Netherlands
Phone: +31 40 277 4000
Fax: +31 40 274 6400
E-mail: karin.vannisselrooij@imec.be

Contributed to this issue

Johan Bauwelinck, Guy Beaucarne, Eric Beyne, Matty Caymax, Mercedes Crego Calama, Bart De Mey, Vladimir Leonov, Kurt Ronse, Jef van de Molengraft, Jan Van Houdt, Werner Verhelst

IMEC vzw – Register of Legal Entities Leuven
VAT BE 0425.260.668 – Kapeldreef 75,
B-3001 Leuven, Belgium

DISCLAIMER

www.imec.be/disclaimer

The entire content of this publication is protected by copyright, full details of which are available at IMEC. All rights reserved. No part of this publication may be reproduced, stored in a retrieval system or transmitted in any form or by any means – electronic, mechanical-photocopying, recording or otherwise – without prior permission of the copyright owner.

Contact person: Katrien Marent – Phone: +32 16 281 880
E-mail: Katrien.Marent@imec.be

Events

- WOCSDICE 2008 – 32nd Workshop on Compound Semiconductor Devices and Integrated Circuits

  May 18-21, 2008, IMEC, Leuven, Belgium

  The 32nd edition of WOCSDICE is organized by IMEC as a forum where researchers can jointly discuss the latest results and trends in the field of compound semiconductor technology and science. This year special emphasis is on III-V compounds and large-area scaling, III-nitride materials, devices and circuits, high-frequency circuits and optical interconnects. The focus will be extended towards organic semiconductors.

  More information: www.wocsdice2008.org

- ECTC2008 – Electronics Components and Technology Conference – Booth #519

  May 27-30, 2008, Disney's Contemporary Resort, Lake Buena Vista, Florida, US

  The premier international packaging, components and microelectronic systems technology conference, ECTC, offers its attendees an outstanding array of packaging technology information. Visit IMEC at booth #519 and learn how IMEC's latest developments in advanced 3D packaging technology provide a solution for today's system integration challenges.

  More information: www.ectc.net

- ALD2008 – 8th International Conference on Atomic Layer Deposition

  June 29-July 2, 2008, Bruges, Belgium

  The AVS Topical Conference on Atomic Layer Deposition is dedicated to the science and technology of atomic layer deposition (ALD) of thin films. The conference will consist of a three-day meeting with a technical program preceded by a workshop in which both basics and future perspectives of ALD will be addressed. Erwin Kessels, Assistant Professor at the University of Eindhoven (The Netherlands) and Annelies Delabie, PhD, Senior Scientist at IMEC, will be the conference chairs.

  More information: www.ald-avs.org

- SEMICON West 2008 – Booth #851

  July 15-17, 2008, Moscone Center, San Francisco California

  SEMICON West is the place to see the companies, technologies and people driving the future of micro- and nanoelectronis design and manufacturing. In 2008, SEMICON West will spotlight technology themes including semiconductors in transition, the mobile electronics revolution and integration of design, production and test. Join IMEC at Semicon West and learn more about IMEC's research on sub-32nm CMOS, heterogeneous integration and advanced packaging, including 3D integration.

  More information: semiconwest.semi.org

- EU PVSEC – 23rd European Photovoltaic Solar Energy Conference and Exhibition – Booth #3/B 8

  September 1-5, 2008, Feria Valencia, Valencia, Spain

  EU PVSEC is the most important international conference in the field of photovoltaics. The international collaboration, which the EU PVSEC facilitates, is essential in fostering a sustainable future for PV technology in the global energy system. During the exhibition, you can visit IMEC and discover recent progress made in bulk-Si solar cell (i-PERC and next generations), thin-film Si solar cell, organic solar cell, III-V solar cell and Ge thermophotovoltaic cell technology.

  More information: www.photovoltaic-conference.com

- UCPSS 2008 – 9th International Symposium on Ultra-Clean Processing of Semiconductor Surfaces

  September 22-24, 2008, Bruges, Belgium

  The Symposium on Ultra-Clean Processing of Semiconductor Surfaces is a biannual event that aims to increase the level of understanding on ultra-clean processing technology in all steps of the IC production. Paul Mertens, manager of IMEC's program on contamination control, cleaning and surface preparation, will be the conference chairman.

  More information: www.ucpss.org

- 5th International Symposium on Immersion Lithography Extensions – Call for papers

  September 22-25, 2008, The Hague, The Netherlands

  You are invited to join other industry experts from around the world in presenting new and unique research results. Now in its fifth year, this symposium continues to focus on the progress in 193nm high-index immersion lithography, double patterning and other extensions to optical lithography, and to build consensus on how the industry will address emerging critical issues. IMEC, in cooperation with SEMATECH and Selete, will host this year's Immersion Symposium.

  More information and call for papers: www.sematech.org/meetings or immersion.symposium@imec.be

- ARRM 2008 – IMEC Annual Research Review Meeting 2008

  October 16-17, 2008, Radisson Sas Royal Hotel, Brussels, Belgium

  IMEC's highly valued annual forum is the place to be for industry executives and research managers to discuss the technological challenges we are facing the coming years. Plan your participation at ARRM 2008 today.

  More information: www.arrm.be