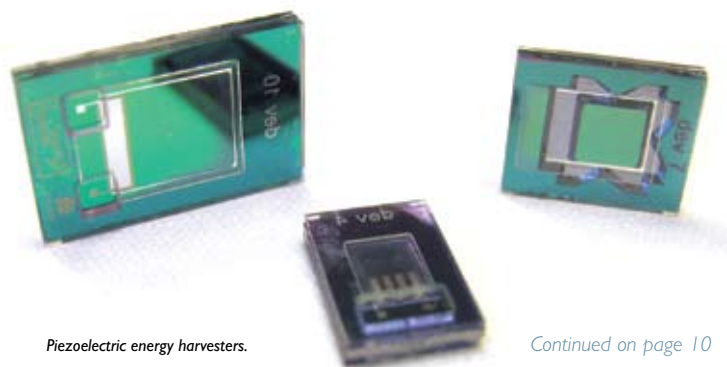


NEWS
FLASH

IMEC reports a micromachined piezoelectric energy harvester delivering 60 μ W

In the framework of Holst Centre, IMEC has further improved its micromachined piezoelectric energy harvester. The device now delivers an output power of 60 μ W, which is a new record for micromachined energy harvesters. Other improvements include the use of aluminum nitride (AlN) as piezoelectric material, allowing a simpler production process, and a lower resonance frequency, making the harvester applicable in more environments. The output power of 60 μ W is sufficient to drive simple wireless sensors that intermittently transfer sensor readings to a master. Potential applications include tire pressure monitoring systems (TPMS) or temperature monitoring of industrial equipment.



Piezoelectric energy harvesters.

Continued on page 10

NEWS
FLASH

IMEC demonstrates 3D stacked integrated circuits

IMEC has made significant progress with its 3D-SIC technology. It recently demonstrated the first functional 3D integrated circuits obtained by die-to-die stacking using 5 μ m Cu through-silicon vias (TSV). It will now further develop 3D-SIC chips on 200mm and 300mm wafers, integrating test circuits from partners participating in its 3D Integration research program.

IMEC reported a first-time demonstration of 3D integrated circuits obtained by die-to-die stacking and using 5 μ m Cu TSVs. The dies were realized on 200mm wafers in IMEC's reference 0.13 μ m CMOS process with an added Cu-TSVs process. For stacking, the top die was thinned down to 25 μ m and bonded to the landing die by Cu-Cu thermocompression. IMEC is upscaling the process for die-to-wafer bonding and is on track for migrating the

process to its 300mm platform. To evaluate the impact of the 3D-SIC flow on the characteristics of the stacked layers, both the top and landing wafers contained CMOS circuits. Extensive tests confirmed that the performance of the circuits does not degrade with adding Cu TSVs and stacking. And to test the integrity and performance of the 3D stack, ring oscillators with varying configurations were made, distributed over the two chip layers and con-

nected with the Cu TSVs. Tested after the TSV and stacking process, these circuits demonstrated the excellent integrity of the chip.

"With these tests, we have demonstrated that our technology allows designing and fabricating fully functional 3D-SIC chips. We are now ready to accept reference test circuits from our industry partners," commented Eric Beyne, IMEC Scientific Director for 3D Technologies, "This will enable the industry to gain early insight and experience with 3D-SIC design, using their own designs".

Editorial

This year, trade publications have been reporting, almost weekly, about semiconductor companies that broaden their activities and enter new markets. Admittedly, some of the larger players will go on scaling for many years to come. But for others, the cost of research and development of next-generation scaling is becoming prohibitive. And others still, are moving into end-user electronics and integration, instead of pure chip technology. As a result, we see a growing interest in technologies such as advanced packaging, photovoltaics, and biomedical electronics.



IMEC has a solid reputation, mainly as a worldwide center of excellence in semiconductor scaling. We have won that position thanks to the unique combination of our three strengths: a team of world-class scientists and engineers, an advanced equipment park, and top partners from the IC industry.

But we are also active in other areas of research – combining electronics with other technologies, for new applications, and in novel ways. We have excellent scientists seasoned in these fields, and we can leverage our expertise in semiconductor technology and our unique, state-of-the-art labs. In solar cell energy, for example, IMEC has a track record of almost 25 years of research. And last year, we reported world-record conversion rates for some of the technologies we investigate. But until recently, the solar cell market was not mature, and there was little interest from industry to collaborate in world-class research. Now the demand for solar cells is growing spectacularly, and many semiconductor companies are looking to gain a share of the solar market.

We thus feel that the momentum is building to expand the other research areas in which we are active, areas such as packaging technology, solar cell technology, MEMS, photonics, and biomedical electronics. Also for these areas, we aspire to excel worldwide and to offer unique R&D collaborations. We are thus ready to welcome – also for these technologies – the third pillar of our success formula: the top partners.

The interest to expand electronics research into new domains is also showing in the initiatives taken by the European Commission. These initiatives, and the strategy behind them, match the IMEC vision. Together with industrial partners, we will cooperate and participate to make this research a success.

IMEC will expand and strengthen its international presence. To be excellent in different research domains, we have to join strengths. And finding the right people and the right research partners is essential to offer unique research programs. We first realized that vision by setting up Holst Centre in the Netherlands together with the Dutch research center TNO, which has a unique expertise in systems-in-foil. The combination of IMEC's research in wireless sensors and the systems-in-foil research enables exciting applications. With Holst Centre, we are present close to companies – such as ASML and Philips – that can benefit from our research. At Holst, we also profit from the infrastructure at the Eindhoven High-Tech Campus. And with IMEC Taiwan, we took a second step to enlarge our international footprint. There also, housed in an R&D center, in the neighborhood of the Taiwanese semiconductor players, we intend to grow, building on our strengths and those of our partners.

Next year – 2009 – we'll celebrate IMEC's 25th year. For that happy occasion, we'll organize a host of events that will be announced in this and future newsletters. There is one special event, though, to which I already draw your attention: in 2009, IMEC's ARRM will take place on June 3 and 4 in Brussels.

Gilbert Declerck, CEO IMEC

#29/in.tangible/scape.s, the new inspiration book by Addictlab and IMEC

In October 2008, IMEC and Addictlab launch a new inspiration book that presents a global approach of science and high-tech applied to arts and design in the wider sense. With this project, IMEC moves one step further in informing and involving as many people as possible in the field of emerging technologies.

#29/in.tangible/scape.s is the result of a collaborative project where research groups and design centers worldwide have developed innovative applications of emerging technologies in the field of art, design, architecture, fashion, communication, environments, health and well-being. In this project, creative thinking has been brought in contact with other ideas from creative minds from completely other fields, with a focus on the emerging invisible (a-material) production. The Addict Inspiration Book #29 is the second publication resulting from

the Addict & IMEC partnership. In a successful first collaboration, visual, conceptual and more practical ways of communicating about nanotechnology have been researched.

For IMEC, the collaboration with Addictlab is a means of increasing creativity and trigger new research opportunities. But even more importantly, it is a way of creating a true dialogue on science, technology, possible applications and implications. It is an ideal bridge to foster cross-

disciplinary exchanges and spread out scientific and technologies development. Because informing society and entering into a dialogue with a variety of communities should become an essential part of all technological development.



Index

EDITORIAL	2
TECHNOLOGY REPORTS	
Calculating hole mobility in Ge and GaAs p-channels with SiO ₂ insulator	4
6nm thin floating gate extends NAND Flash to 22nm technology node	5
IMEC confirms strategy for crystalline Si solar cells	6
IMEC reports ideal candidate transistor for high-power switching	7
IMEC presents scalable architecture for flexible FEC	9
IMEC integrates SDR-enabling technology	9
NEWSFLASHES	
IMEC reports a micromachined piezoelectric energy harvester delivering 60µW	1
IMEC demonstrates 3D stacked integrated circuits	1
#29/in.tangible/scape.s, the new inspiration book by Addictlab and IMEC	3
IMEC starts new research activities on resistive RAM	5
IMEC and Plextronics collaborate on high-efficiency reproducible organic solar cells	6
Toshiba licenses IMEC's power-efficient, flexible processor technology	8
First steps towards wireless ambulatory emotion monitoring	10
IMEC IRIS-1 sensor revives in 'Mars Webcam'	12
INDUSTRY LINK	
eHealth closer to reality thanks to real-time relevant medical data extraction	11
EUROPEAN PROJECTS	
IMEC and CEA-LETI gear up cost-effective silicon photonics prototyping service	12
IMEC embeds active optical links in flexible substrates	13
COURSES	8
PATENTS	13
AWARDS	14
EVENTS	14
COLOPHON	15

Calculating hole mobility in Ge and GaAs p-channels with SiO₂ insulator

IMEC in collaboration with the University of Massachusetts, USA, has computed the hole mobility in Ge p-channel and, for the first time, in GaAs p-channel inversion layers with a SiO₂ insulator. These results are important to further evaluate the feasibility of using Ge and GaAs semiconductors for 'beyond Si' scaling. Computations are based on the results of subband structure calculations which, in turn, are done using an improved self-consistent method.

Ge and several III-V compound semiconductors are being considered as a means to push transistor scaling 'beyond Si'. While this is understandable for n-channel devices, the picture is less clear for p-type inversion channels. For these devices, the hole transport properties are less known and not manifestly superior to Si. Ge and some III-V materials exhibit large bulk hole mobilities, so it is crucial to understand whether or not a superior performance is retained in inversion layers.

IMEC and the University of Massachusetts have therefore calculated the hole mobility in Ge and GaAs p-channel inversion layers with a SiO₂ insulator. Various scattering mechanisms, i.e., the acoustic/optical phonon scattering, surface-roughness (SR) scattering and longitudinal-optical (LO) phonon scattering (for GaAs only) have been taken into account. For SR scattering, also the static screening effect has been included. This degrades the scattering strength and thus enhances the hole

mobility, especially for the strong inversion case. Relaxed as well as biaxial strained p-channels have been investigated.

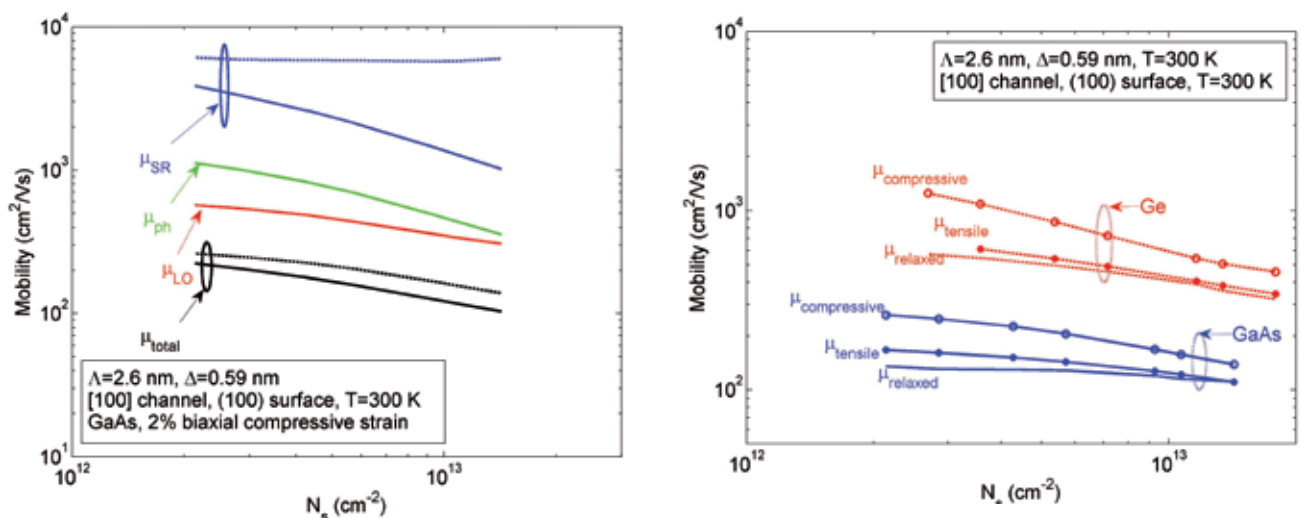
The mobility calculations have been based on computations of the subband structure of the p-channels. This task is quite challenging, since the non-parabolic, warped and anisotropic nature of the valence bands renders effective mass approximations questionable and requires the use of more sophisticated band-structure models. Therefore, an improved self-consistent method was developed. The method consists in solving the coupled Schrödinger and Poisson equations iteratively. The Schrödinger equation is solved in the framework of the six-band $k \cdot p$ method using finite differencing on an inhomogeneous grid. Compared with previous methods for valence band structure calculation in p-channel inversion layers, this improved method is more straightforward and easier to implement with high efficiency and satisfied accu-

racy. The improved method has been validated using a general self-consistent method.

For the Ge case, the results of the mobility calculations have been compared with experimental data and good agreement has been found. For III-V, to our knowledge, no published results exist and therefore, hole mobilities in both relaxed and biaxial strained GaAs p-channels are presented for the first time. The results show that the Ge p-channel exhibits a hole mobility about four times larger compared with the GaAs p-channel. Simulation results also demonstrate that biaxial compressive strain is most effective in increasing the hole mobility.

In the future, calculations will be extended for p-channel inversion layers with a high-k insulator, which introduces an extra scattering mechanism named the remote phonon or surface optical (SO) phonon scattering.

These results have been presented at the 2008 European Solid-State Device Research Conference (ESSDERC).



Hole mobility in 2% biaxial compressive strained (left) GaAs p-channels and comparison with results in Ge p-channels (right). The dashed line represents the mobility with static screening, and the solid line is for unscreened results.

6nm thin floating gate extends NAND Flash to 22nm technology node

By thinning the floating gate (FG) to a thickness as low as 6nm, IMEC could drastically reduce the electrical interference between adjacent memory cells and hence overcome one of the main limitations for further FG-based NAND Flash scaling. A key solution for achieving such a thin FG was the use of ASM's Silcore® process for Si deposition in an A412™ vertical furnace.

When scaling FG-based NAND-Flash technology below the 45nm node, planarization of the memory cell structure is needed because the control gate (CG) can no longer be wrapped around the FG. The resulting loss in capacitive coupling between CG and FG is then solved by introducing a high-k material in the interpoly dielectric (IPD) stack. However, electrostatic interference between adjacent cells remains one of the main challenges for further downscaling.

One possible way to tackle the interference problem is to decrease the thickness of the FG layer. While state-of-the-art FG Flash is currently using a 60nm thick FG, simulations have shown that a decrease of the FG thickness below 20nm drastically reduces the interference between adjacent cells. E.g., for the 22nm technology generation, an acceptable CG to FG coupling ratio of 50% can

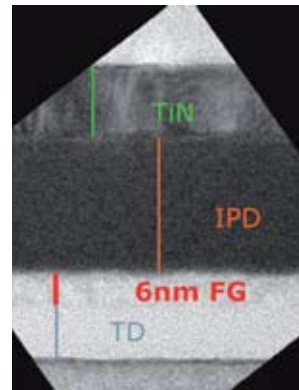
be obtained for a 5nm FG. With the commonly used silane-based Si depositions for FG, it is however not possible to achieve well controlled thin layers below 25nm. Therefore, Silcore®, an ASM proprietary version of purified trisilane Si_3H_8 , was used as a precursor for Si deposition. The main advantage of this precursor for FG memory applications is the ability of depositing very thin, smooth and uniform Si films.

To demonstrate the memory operation with a Silcore®-based FG of only 6nm thick, stacked gate capacitors were fabricated with a 8.5nm tunnel oxide, a 17nm Al_2O_3 IPD stack and TiN/poly CG. Excellent program (P) and erase (E) per-

formance was observed (with program levels of 2V above the intrinsic level) in combination with very good endurance and data retention (after 10^5 P/E cycles).

These results show that by aggressively decreasing the thickness of the FG to 6nm, the FG-based NAND Flash technology can be extended to the 22nm generation, hence having a much longer life span than predicted. This allows delaying the transition to the charge trapping (CT) memory concept which was marked out as a candidate for

the sub-40nm node. Although CT does not suffer from electrostatic interference, the concept is still far from mature and faces some major drawbacks like smaller P/E window, lower erase speed and worse retention time.



Cross-section transmission electron microscopy picture of the FG memory capacitor with a Silcore®-based FG of only 6nm thick.

NEWS FLASH

IMEC starts new research activities on resistive RAM

News from IMEC's (sub-)32nm research platform

In order to explore solutions to overcome the scaling limitations of conventional Flash memory cells, IMEC has started new research activities on resistive RAM (RRAM) cells. With these activities, IMEC answers the needs of today's major memory companies.

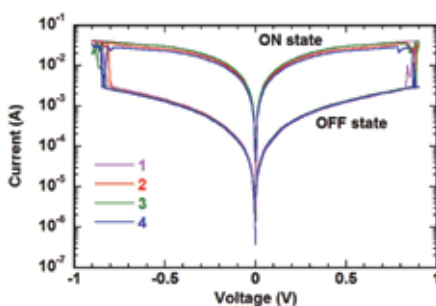
Resistive switching memories are based on materials whose resistivity can be electrically switched between high and low conductive states. RRAM is becoming of interest for future scaled memories because of their superior intrinsic scaling character-

istics compared to the charge-based Flash devices, and potentially small cell size (enabling dense crossbar RRAM arrays using vertical diode selecting elements). The latter will allow the ultimate cell size of $4F^2$ (with F the technology minimal feature size, i.e., half the metal pitch). RRAM is seen as a potential candidate to replace conventional Flash memory and hence to push NVM technology towards the (sub-)22nm technology node.

For making such RRAM, different concepts and materials are proposed. The IMEC research activities on RRAM mainly focus on investigating the switching behavior of the RRAM cell concept that uses metal oxides as a switching element, and on demonstrating its scaling capability down to 25nm. The

study concentrates on three main topics, being RRAM stack optimization (including the choice of top and bottom electrode and of the metal oxide), RRAM cell scaling and RRAM integration in a crossbar RRAM array.

These new research activities are part of IMEC's Emerging Memory program that provides innovative non-volatile memory (NVM) technology, concepts and solutions for the 32nm generation and below. Besides activities on RRAM, IMEC also started to explore floating body cells (FBCs) for embedded and stand-alone DRAM and SRAM replacement. With these activities, IMEC answers the needs of today's major memory industry players. IMEC's vast background in NVM memory physics, reliability, modeling as well as process integration in state-of-the-art platforms and design and test issues, allows for these new concepts to be explored in a fast and cost-effective way.



Resistive switching in an experimental metal oxides (MOx) RRAM element.

IMEC and Plextronics collaborate on high-efficiency reproducible organic solar cells

IMEC and Plextronics, Inc., an international technology company specializing in printed solar, lighting and other organic electronics, signed an agreement to collaborate on state-of-the-art materials and inks for organic solar cells.

With this collaboration, IMEC aims to develop a reproducible process for high-efficiency organic solar cells using Plextronics' Plexcore® branded materials and inks, which have demonstrated world-record efficiencies as high as 5.9%, according to recent testing at the National Renewable Energy Laboratory (NREL) in Colorado.

IMEC aims to develop organic multi-junction solar cells with efficiency of 10% by 2012. IMEC's focus

is also on up-scaling of the process to achieve a large-area industrial manufacturing technology with an average efficiency of 7% (+/- 0.5%) and solar cell lifetime of 5 years.

To realize these goals, high-quality, highly reproducible commercial materials are essential. In the first phase, IMEC will investigate Plexcore® OS, which is a regioregular poly-3-hexylthiophene (P3HT) polymer with a high absorption coefficient close

to the maximum photon flux in the solar spectrum and high mobility. Plexcore® OS materials will be processed using spin coating and validated on film morphology, carrier mobility and reproducibility. Solar cells will be processed on different substrates using spin-coated films of the material.

Future research will include evaluation of other Plexcore® materials and inks, using deposition techniques such as screen and inkjet printing and spray coating on large-area substrates.

IMEC confirms strategy for crystalline Si solar cells

Crystalline Si will remain the material of choice for solar cells in the next decade. Still, for the market to remain growing at today's rate, the cost of the cells will have to come down considerably, and the efficiencies will have to improve. IMEC is pursuing these goals, developing the next generations in both wafer-based bulk silicon solar cells and epitaxial cells.

Today, the photovoltaic market is growing at an annual rate of 40%. In that market, crystalline Si solar cells have a share of over 90%. The growth of the photovoltaics market and the dominance of crystalline Si as material are expected to go on for at least another decade. But to reduce the cost of the energy generated with Si solar cells, the industry still has to take some important hurdles. The amount of Si that is used per Wp should be reduced by at least a factor of 2. And the efficiency of the solar cells should be increased by 25%, going from 16% to over 20% for industrial crystalline Si solar cells. The other components of the solar cells, such as the metallization layers, surface and contact passivation, should be produced more efficiently and with cheaper materials. And last, there is the challenge to bring the production costs down, for example by using larger wafers or by producing in larger facilities with a manufacturing throughput in the order of a GW/year.

Since IMEC started working on solar cells, back in 1984, the R&D on crystalline Si solar cells has formed the backbone of its photovoltaic activities. And although other options are also investigated, the R&D on crystalline Si solar cells still forms an important part of IMEC's photovoltaic research.

Today, IMEC explores both wafer-based bulk silicon solar cells and epitaxial cells. For bulk silicon solar cells, IMEC develops the generic process technology needed to increase the efficiency and to reduce the manufacturing cost of solar cells. There is a roadmap to reduce the active silicon layer thickness from 150µm today down to 40µm in 2020. And to reach efficiencies of up to 20%, IMEC develops alternative back-side dielectric passivation layers, selective doping of emitter and back surface contacts, novel metallization technologies, and interdigitated back-side contacts (i-BC). These techniques will then be integrated in novel industrial process flows.

In addition, IMEC investigates the integration of cells into modules, which becomes more challenging with thinner wafers. We will also further work on solar cell reliability, as the guaranteed lifetime of cells and modules will increase from 20-25 years up to 35 years and more in the next decade. And we will

look into new methods to handle wafers as thin as 40µm. The potential of the innovations will be benchmarked with both small-area lab cells and large-area solar cells.

Next to the generic bulk silicon research, which is important for any crystalline silicon wafer-based solar cell technology, epitaxial thin-film (<20µm) silicon solar cells on low-cost silicon carrier will also be developed. Epitaxial thin-film silicon solar cell technology is expected to be the intermediate step before mainstream fabs will switch from bulk silicon solar cells to thin-film solar cells. The process is generically similar to the bulk process and the epi-process can be implemented with limited equipment investment. To improve the optical confinement of light in the active part of the cell, a highly efficient buried porous Si reflector will be integrated in the solar cell structure.



Large-area thin-wafer Si solar cell.

IMEC reports ideal candidate transistor for high-power switching

By using AlGaN/GaN/AlGaN double heterostructures grown on 4-inch Si substrates, IMEC has demonstrated breakdown voltages as high as 650V. The devices have small (5-8 μm) gate-drain distance and low transistor on-resistance. These results make the AlGaN/GaN/AlGaN double heterostructure field-effect transistor (DHFET) an ideal candidate for high-power switching applications.

AlGaN/GaN-based HFETs are obvious candidates for high-power switching applications because of the high breakdown field and low transistor on-resistance (R_{on}). Although high breakdown voltages have been reported for epilayer growth on SiC or sapphire substrates, large-diameter Si substrates are preferred since they offer a lower-cost technology. Recently, high breakdown voltages have been reported on AlGaN/GaN single heterostructure devices (SHFETs) fabricated on Si.

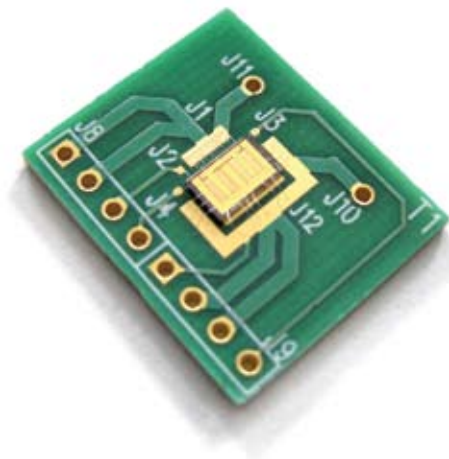
Alternatively, IMEC has investigated the breakdown behavior of AlGaN/GaN/AlGaN double HFETs grown on 4-inch Si substrates. Such devices are characterized by an extremely low leakage current due to both the electron confinement in the GaN channel and the high bandgap of the AlGaN buffer. IMEC has recently demonstrated successful growth of these structures and has optimized the

thickness, composition and growth conditions for power switching applications.

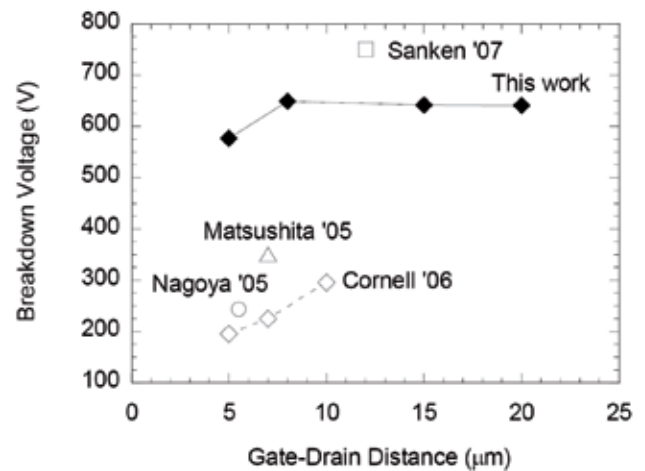
The epitaxial growth on 4-inch Si substrates starts with an AlN layer, followed by an AlGaN buffer layer stack and a thick AlGaN layer. The DHFET epistuctures are completed by the growth of a GaN channel, 25nm $\text{Al}_{0.35}\text{Ga}_{0.65}\text{N}$ and an in-situ grown Si nitride passivation layer. The total thickness of the buffer layer is varied up to 2.7 μm . Studies of the horizontal and vertical AlGaN buffer breakdown show a linear dependence on the epitaxial buffer layer thickness. The presence of a thick buffer layer is believed to suppress the buffer leakage current and hence to enable a high breakdown voltage. The vertical breakdown field is estimated to be 1.6MV/cm, only a factor of 4 below the theoretical limit.

To achieve high device breakdown voltages, FETs were processed on a double heterostructure epilayer with a total buffer thickness as high as 2.7 μm . This buffer layer stack has a buffer breakdown of 800V. Devices with 1.5 μm gate length, 1.5 μm source-gate distance and 200 μm gate width were fabricated; the gate-drain distance (L_{gd}) varied between 5 and 20 μm . The breakdown voltage is as high as 575V for 5 μm L_{gd} and saturates at a value of 645V for L_{gd} equal or higher than 8 μm . A transistor on-resistance value as low as 7.2 Ωmm was obtained for 5 μm L_{gd} .

Benchmarking data show that these are the highest breakdown voltage values reported so far for small gate-drain spacings. For these high device breakdown values, the specific on-resistance is more than an order of magnitude lower than the theoretical breakdown limit for unipolar Si devices. These results clearly demonstrate the superior properties of DHFET devices for use in power switching applications.



DHFET power transistor mounted on a measurement PCB.



Relation between breakdown voltage and gate-drain distance for the fabricated DHFETs compared with state-of-the-art SHFETs on Si.

Prof. Gilbert Declerck, CEO of IMEC, was honored with the European SEMI Award 2008 for leading IMEC to become one of the world's most prestigious independent microelectronics research institutes. The award was presented at the SEMI Executive Summit at SEMICON Europa in Stuttgart, Germany.

> More awards: see page 14.

Toshiba licenses IMEC's power-efficient, flexible processor technology

Toshiba, world-leading integrated device manufacturer, has licensed IMEC technology for designing power-efficient, flexible processors in a single- and multiprocessor architecture. The agreement concerns IMEC's ADRES reconfigurable processor template, the DRESC compiler, and the MPSoC suite of design tools. Toshiba will also cooperate with IMEC to develop processors and tools that enable gigabit/s demodulation.

ADRES (Architecture for Dynamically Reconfigurable Embedded Systems) is a processor architecture designed for wireless and multimedia processing in single- and multiprocessor systems. ADRES processors are suited for future mobile terminals, such as software-defined radios. They combine state-of-the-art power efficiency, excellent performance, and flexibility.

Through an XML template, designers can create the ADRES processor instance that is best suited for their applications. And applications for an ADRES processor can be completely programmed in a high-level programming language (C) and compiled with the DRESC compiler, included in the license. This is of key importance for short time-to-market.

MPSoC is a suite of tools to help build and map applications for multiprocessor platforms. The

suite's first toolset, called CleanC, allows designers to write sequential, high-level code that is optimized for parallelization. The second toolset then enables mapping the sequential C code on a multiprocessor platform. MPSoC relieves the designers of having to code synchronization, data communication between threads, and memory organization. Thanks to the parallelization tools, for instance, several multithreaded versions of the same application can be explored in a short time. This greatly reduces the application complexity and design time, enabling designers to bring multiprocessor-based embedded-system platforms faster to the market.

"Before entering into this agreement, Toshiba thoroughly evaluated the IMEC technology. It then decided not only to license ADRES and MPSoC, but also to cooperate with IMEC to develop processors and tools that enable gigabit/s demodulation. This

testifies that IMEC's research into efficient embedded multiprocessor systems is world-class", said Rudy Lauwereins, Vice President Nomadic Embedded Systems at IMEC.

"We are confident that IMEC's dynamic reconfigurable processor technology will bring significant advantage to the development of our wireless base-band SoCs in terms of design time, flexibility and area," said Tohru Furuyama, General Manager of Center for Semiconductor Research & Development at Toshiba. "We are looking forward to collaborating with IMEC which will allow us to leverage on the expertise and knowledge of IMEC's research team and enable us to also provide valuable technologies and products to our customers."

More information on ADRES:

http://www2.imec.be/imec_com/adres-reconfigurable-processor-template.php

More information on MPSoC tools:

http://www2.imec.be/imec_com/mpsoc_methods_tools.php

Courses

An overview of upcoming courses, organized by IMEC's training center MTC:

- **Variability-aware modeling and yield aspects**
October 27, 2008, IMEC, Leuven, Belgium
- **Design of experiments – introductory course**
November 3, 17, 18 and December 1, 2008, IMEC, Leuven, Belgium
- **Bottom-up and top-down nanotechnology**
November 12-14, 2008, IMEC, Leuven, Belgium
Organized by MTC and Marc Madou, University of California, Irvine, US
- **Co-fabrication of MEMS and electronics**
December 8-9, 2008, IMEC, Leuven, Belgium
- **Adhesion science and technology**
December 8-9, 2008, IMEC, Leuven, Belgium



The Center for Advanced Learning in Information Technologies (CALIT) announces the advanced course:

- **TAD: Avoidance versus adaptability for variability and its time dependency**
November 25, 2008, IMEC, Leuven, Belgium

More information and a full overview of courses: www.imec.be/mtc

News from IDESA

MTC is prime contractor for IDESA, a project in the EC 7th Framework Program. IDESA's goal is to support universities to keep up with the evolution of the IC design and implementation flows for deep submicron technologies. In the months to come, the project offers the following training courses at different sites in Europe:

- **IDESDA Digital**, October 27-31; November 24-28 and February 16-20, 2008
- **IDESDA Design for Manufacturing**, November 4-7, 2008
- **IDESDA RF**, December 1-5, 2008
- **IDESDA Analog**, December 8-12, 2008

More information: www.idesa-training.org



IMEC presents scalable architecture for flexible FEC

IMEC has developed an innovative architecture for flexible forward error correction (FEC). The solution targets data transmission applications that need to combine flexibility, high throughput, and low power consumption. Examples are future wireless terminals and optical storage. IMEC's FEC enables, on one processor, the turbo- and LDPC (low-density parity check) decoding of major communication standards. The technology is available for the industry either through a soft IP transfer, or through joint R&D projects.

IMEC's FEC solution supports both turbo- and LDPC coding, including multi-channel operation over different modes. It is the world's first application-specific integrated processor (ASIP) for flexible FEC enabling both turbo- and LDPC coding for 3rd generation mobile phones (3GPP-LTE), wireless networks (IEEE802.11n, IEEE802.16(e)) and television broadcasting (DVB-S2/T2, GB20600). Support for other convolutional turbo- or LDPC codes can be enabled through assembly programming. A combined multiprocessor and ultra-wide SIMD (single instruction, multiple data) approach achieves scalability, high throughput and high energy efficiency.

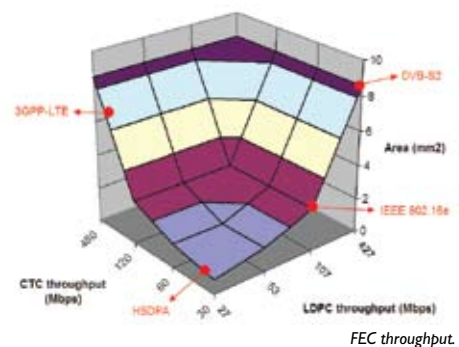
The preliminary estimates for throughput and energy consumption show that IMEC's FEC solution is competitive with solutions that separate turbo and LDPC decoding on dedicated hardware. The throughput that is achieved is between 0.07 and 1.25Mbps/MHz,

with efficiencies from 0.3 to 0.5nJ/bit/iter in turbo mode and 0.08 to 0.1nJ/bit/iter in LDPC mode. The silicon area used by the flexible solution is comparable to the sum of multiple dedicated solutions.

The new flexible FEC fits in IMEC's research strategy to design flexible components for data transmission. These are targeted at, amongst others, future mobile terminals; they combine high throughput, low power consumption, and a small footprint. Other IMEC components that follow this vision are a flexible RF transceiver and a flexible baseband chip. IMEC invites partners to collaborate in this research through its joint research programs. Industrial players can also profit from IMEC's research by licensing the components.

FEC is used in all digital transmitters and receivers to ensure that the digital message is sent

free of errors. When the transmitter sends a message, it encodes the bit stream, adding redundant data. These allow the receiver to detect and correct errors - within some bounds - without asking the transmitter for additional data. State-of-the-art FEC mainly uses 2 methods of FEC coding: turbo codes and LDPC codes. These are popular because they allow high-speed FEC encoding and decoding. But turbo codes and LDPC codes are complex, and decoding them puts a heavy computational load on the receiver. Therefore, until recently, FEC decoders for the different FEC methods were implemented as dedicated hardware blocks, focusing on minimum power consumption and area, and thereby sacrificing flexibility.



IMEC integrates SDR-enabling technology

IMEC has integrated its key innovative components for next-generation flexible mobile terminals. The prototype wireless setup, with IMEC's flexible RF transceiver and programmable baseband platform, proves the conceptual integrity of the SDR solution and the compatibility of the enabling components. It is now possible to measure the actual performance and power consumption in real-life conditions and for different operating modes. This will validate the unique capabilities of the technology.

Flexible RF transceiver – SCALDIO

IMEC's flexible RF transceiver front-end, codename SCALDIO, operates with all current and future cellular, wireless local area network (WLAN), wireless personal area network (WPAN), broadcast and positioning standards in the frequency range between 174MHz and 6GHz.

SCALDIO includes a fully reconfigurable direct-conversion receiver, transmitter and two synthesizers. Its configuration knobs tune the power and frontend characteristics (such as the RF carrier frequency, channel bandwidth, noise figure, linear-

ity, filter characteristic) to the requirements of the standards that are used. SCALDIO uses innovative mixed-signal control, calibration and compensation techniques to relax the specifications in the analog domain.

Its innovative architecture has a power consumption and CMOS chip area comparable to current state-of-the-art single-mode radio front-ends. Its performance, power, and cost requirements make it suited for next-generation mass volume mobile devices.

Programmable baseband platform – BEAR

IMEC's programmable baseband platform is ready to support next generations of mobile devices featuring standards such as 802.11n, 802.16e, and mobile TV. And it is forward compatible with the upcoming 3GPP-LTE communication standard. The heterogeneous multi-processor system-on-chip (MPSOC) baseband platform achieves both functional flexibility and energy efficiency through

opportunistic partitioning. The platform features a digital baseband front-end (DFE) implementing the packet detection. This DFE includes a synchronization processor, which is a dedicated ASIP programmable in assembly. The remainder of the platform, which is heavily duty cycled, consists of two baseband processors for data processing and an ARM926 for event-based control flow, inter-core data transfer, and MAC. For the baseband processor, two optimized instantiations of IMEC's ADRES core are included.

- RF tuning range: 100 MHz - 6GHz
- Signal bandwidths supported: 1MHz - 40 MHz
- Digital 0.13µm CMOS
 - 1.2V supply
 - 7.7 mm²
 - 60-120mW, depending on standard

- TSMC 90G Multi-VT technology
- 32 mm core die area, 20 mm active area
- 6.7 Mbit memory (121 instances)
- 4 power domains, 8 clocks
- 270 I/O pins, 267 supply pins
- 2 ADRES processors, each with:
 - o 33 memory macro @ 400MHz
 - 2 32KByte instruction cache
 - 2 128-entries config mem
 - 2 64KByte data scratchpad
 - o 128KByte IMEM @ 200MHz
 - o 400MHz Clock rate (worst-case commercial)

First steps towards wireless ambulatory emotion monitoring

In the framework of Holst Centre, IMEC has demonstrated the feasibility of using a body area network (BAN) platform to extract a person's arousal response based on physiological signals reflecting autonomic nervous system (ANS) activity. Wireless, low power, miniaturized and in real-time, the system significantly enhances comfort of monitoring and opens new perspectives for e.g. human computer interaction.

Monitoring of a user's emotion state is becoming increasingly popular, with applications in psychophysiology, gaming and human computer interaction. While research in this area has been focusing mainly on discovering patterns within the ANS signals specific to a given emotional state, little emphasis has so far been put on the monitoring hardware. Within its Human++ program at Holst Centre, IMEC has now demonstrated the applicability of using a BAN for the ambulatory monitoring of physiological changes in the ANS.

The BAN consists of two small wireless sensor nodes that provide a platform to which four different kinds of sensors are interfaced. The sensors measure electrocardiography (ECG) signals, respiration, galvanic skin response (GSR) and skin temperature (SkT), respectively. The ECG sensor relies on an IMEC proprietary single-channel ASIC for biopotential read-out. The ASIC is a low-power and high-performance front-end for biopotential applications. GSR is defined as the skin conductance between two locations on the hand, and is measured at constant DC voltage. Commercially available sensors are used to measure respiration and skin temperature. A circuit board containing the GSR circuit and temperature sensor are integrated into a wristband for user comfort;

the piezoelectric sensor for measuring respiration and the ECG electrodes are integrated into a single chest belt.

A high arousal state is typically associated with a short-time feeling of excitement, surprise, fear or discomfort. This can be elicited by appropriate movies, pictures, music or mental exercises. In a typical test set-up, a subject is asked, for instance, to watch a movie clip while her physiological signals are being monitored. Sensor signals are sent wirelessly to a computer, analyzed in real-time and converted to a subset of relevant features. Statistical pattern recognition techniques have led to the identification of four features highly correlated to arousal. These account for heart rate variability, as well as duration, intensity and variability of the galvanic skin response. These four features are then mapped linearly to an arousal level, characteristic of the emotional state of the test subject at this point in time. The experiment demonstrates the applicability of the body area network for the real-time ambulatory monitoring of emotions, in particular arousal. The use of features

extracted from the respiration and skin temperature signals to improve the measurement of arousal is currently under investigation. The small system dimensions and wireless operation enhance the monitoring comfort and user acceptance and enable monitoring of emotional responses out of the lab environment, *on-the-move*. This opens new perspectives for human computer interaction, e.g. in interactive gaming and for applications such as pharmaceutical drug screening. Currently, a study is ongoing to evaluate the technology in a clinical environment.

Upcoming challenges consist in making the system autonomous (by using e.g. energy harvesters); moving the processing unit from the computer to the sensor node; increasing the number of input parameters (so far limited to four); achieving seamless wearable monitoring systems; increasing the system reliability for monitoring *on-the-move* and including ultra-low power wireless RF communication.



Wireless body area network for arousal monitoring: physiological signals are monitored, wirelessly transmitted and analyzed to extract, in real-time, the arousal level characteristic of a person's emotional state.

Continued from p. 1

News from Holst Centre

IMEC reports a micromachined piezoelectric energy harvester delivering 60 μ W

Energy harvesters convert ambient energy – light, heat, or vibrations – into electricity. They are indispensable in situations where batteries cannot be replaced easily. Examples are autonomous sensor networks that are distributed over large areas and in locations that are difficult to access. IMEC's new energy harvester is a micromachined device converting vibration energy through a piezoelectric transducer. It can be used to generate energy for sensors in, for example, planes, vehicles, or vibrating industrial equipment. For the new harvester,

an experimental output power of 60 μ W was measured. The device has a resonance frequency of 500Hz and an acceleration of 2g. It consists of a piezoelectric capacitor formed by a Pt electrode, an AlN piezoelectric layer and a top Al electrode. The capacitor is fabricated on a cantilever which has a mass on its tip. When the harvester vibrates, the mass on the cantilever causes the piezoelectric layer to be stretched, inducing an electrical power. The use of AlN as piezoelectric material makes the device compatible with CMOS processes,

allowing production at a lower cost. Last year, IMEC already showcased a piezoelectric harvester with a reported 40 μ W output power. But this earlier device had a piezoelectric layer fabricated in PZT. The current AlN layer has the advantage that it can be made in a simpler deposition process. Moreover, the PZT device operated at 1.8kHz. The lower resonance frequency of the new harvester – 500Hz – corresponds with vibration frequencies in, for example, industrial equipment or car tires. This greatly enlarges its field of application.

eHealth closer to reality thanks to real-time relevant medical data extraction

IMEC and i.Know apply ‘knowledge streaming’ on wireless cardiac monitoring

In the framework of Holst Centre, IMEC has broadened the functionality and scope of its wireless health monitoring technology by linking it to real-time extraction of relevant medical data. The new technology builds upon the ‘knowledge streaming’ concept of i.Know - a Belgian SME specialized in intelligent applications for automated knowledge extraction and representation. The system takes a central position in the future scenarios of eHealth and personalized medicine.

The rising cost of healthcare in developed countries calls for alternative ways of increasing efficiency, productivity and usability. Future health monitoring systems will deliver intelligent services in chronic disease management, assisted medical diagnostics, patient compliance monitoring and emergency response. In all of these scenarios, the availability and interpretation of personal medical data plays a crucial role.

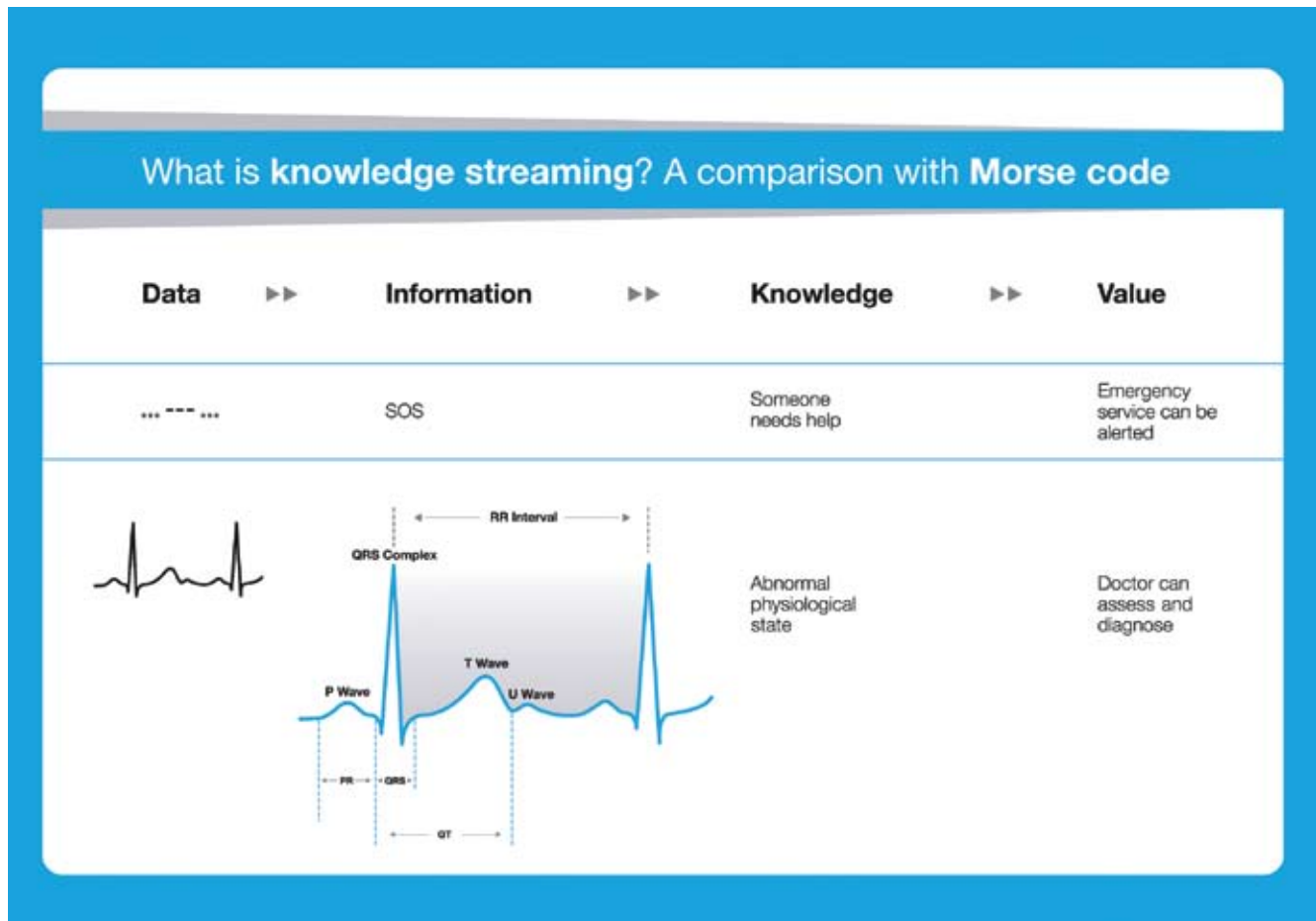
Within its Human++ research program at Holst Centre, IMEC already focuses on building blocks for miniaturized wireless sensor nodes allowing comfortable and continuous measurement of

body parameters. Thanks to the collaboration with i.Know, the Human++ program moves one step further in the chain and also develops technologies that allow fast and accurate interpretation of the collected data.

The technology developed by IMEC and i.Know is illustrated for the case of ambulatory cardiac monitoring (electrocardiography, ECG). Based upon an incoming stream of ECG signals, relevant features are extracted and associated with an objective interpretation. For example the heart rhythm and the shape of an ECG peak allow the system to detect abnormal physiological events. As a consequence, a doctor or a call centre can be

alerted to diagnose the status of the monitored patient.

Now that the concept is proven, IMEC and i.Know will further enhance the system by associating it with external databases such as electronic patient records and PubMed. By doing so, the detection of abnormal events can be enriched with contextual data (such as the medication history of the patient). This will e.g. allow doctors to easier find their way in an abundance of data and support their diagnosis. Future research also targets the integration of data from multiple sensors such as electroencephalography (EEG), electromyography (EMG), physical activity monitoring and temperature, allowing more precise interpretations. The concept of knowledge streaming provides a generic framework for data fusion and context-aware monitoring, possibly applicable in domains other than healthcare and medicine.



Knowledge streaming encompasses the combination of extracting relevant data from abstract signals, assigning an objective interpretation to it and distributing it when necessary, all of this at real time on an incoming signal. Within Holst Centre, IMEC applied the concept for medical data extraction.

IMEC and CEA-LETI gear up cost-effective silicon photonics prototyping service

IMEC and CEA-LETI launch ePIXfab, the continuation of their successful multi-project wafer silicon photonics prototyping service started in 2006. Co-funded by the European Union through the Seventh Framework Program and coordinated by IMEC, ePIXfab aims at reducing the large barriers for access to and market take-up of silicon photonics technology by focusing on reduced cost, risk and design effort, education, and roadmapping.

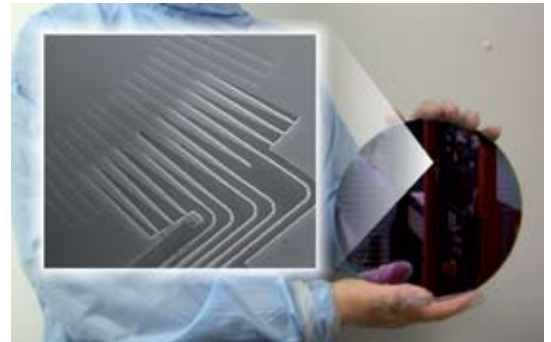
With their joint initiative ePIXfab, IMEC and CEA-LETI continue to offer a cost-effective way for researchers and SMEs (small and medium sized enterprises) to prototype photonic integrated circuits in silicon. ePIXfab organizes shuttle (also called multi-project wafer) fabrication runs with IMEC and LETI wafer-scale technologies, including 193nm deep-UV lithography-based processes. Now, IMEC and LETI have agreed to significantly extend this service to enable a broader market take-up of silicon photonic IC technology. Dedicated prototyping and small-volume manufacturing is also possible based on IMEC or LETI technology.

A wider offer

Starting in September 2008, the PhotonFAB project will provide the ePIXfab service with a more extensive technology portfolio, new design libraries, education and training for the clients, a shuttle

service roadmap and a more streamlined operation. Funded by the European Union as a FP7 Support Action, PhotonFAB will in this way lower the design effort, risk and bare costs for the clients. In addition, clients from countries fully associated to the FP7 program will be able to get additional cost reductions for the shuttle service and training activities.

Silicon photonics IC technology enables versatile and highly functional integrated circuits that handle light information. Photonic integrated circuits are used in applications such as communication networks, sensors, monitoring and bio-analysis. Using silicon allows to increase the functionality of a photonic chip by several orders of magnitude. By manufacturing with CMOS technology, the chips are reliable and can be used in volume applications.



200mm silicon-on-insulator wafer containing more than 100 chips with more than thousands of photonic devices each.

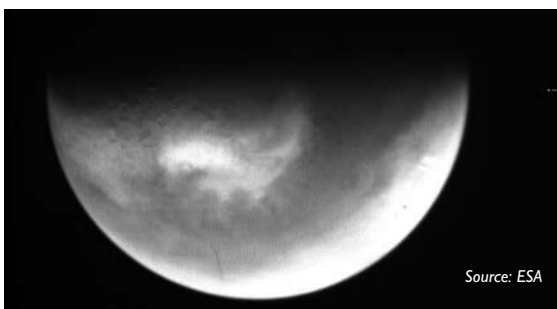
Since 2006, thanks to the collaboration between IMEC and CEA-LETI, over 25 academic and SME groups have been able to perform their research and develop their IC technology in a fabless way with reduced costs, by grouping IC designs in a single fabrication run.

Detailed information on the ePIXfab services is available from www.epixfab.eu.

NEWS FLASH

IMEC IRIS-1 sensor revives in 'Mars Webcam'

The Visual Monitoring Camera (VMC) containing the integrated radiation tolerant imaging system (IRIS)-1 developed at IMEC, has recently been brought in action again as the 'Mars Webcam', providing views not obtainable from earth. The camera is in orbit around Mars since December 2003 as part of Mars Express.



A Visual Monitoring Camera (VMC) is carried on several spacecrafts of the European Space Agency (ESA) to provide visual feedback of the spacecraft

environment. These basic optical monitoring cameras, developed by OIP Sensor Systems (Oudenaarde, Belgium), are all equipped with a CMOS-based sensor. A camera containing IMEC's IRIS-1 integrating CMOS active pixel sensor (APS) was used for Mars Express, ESA's deep-space probe now orbiting the red planet. The VMC was installed on the orbiter with the only purpose of providing simple, low-tech images of the Beagle lander separation from the orbiting Mars probe in December 2003. The single-chip sensor is

capable of producing 640x480 pixel images with 8 bits per sampling depth.

Following three years of inactivity, ESA decided to study the possibility of reviving the IRIS-1 based VMC camera in a completely different role, namely as a 'Mars Webcam'. In its second live with on average 3 observations per week, the VMC is now used for public relations, outreach and auxiliary science data gathering.

Since 2003, 2nd and 3rd generation image sensors have been realized (IRIS-2 and IRIS-3) in collaboration with Fillfactory/Cypress and a new compact VMC camera incorporating these sensors has been developed by OIP.

You can view images of the red planet on www.esa.int/SPECIALS/VMC.

IMEC embeds active optical links in flexible substrates

INTEC, IMEC's associated laboratory at the Ghent University has made the first functional optical links embedded in a flexible substrate. The links include optical waveguides, light sources, and detectors. With this technique, it becomes possible to make foils that sense changes in pressure. Such sensing, skin-like foils could be used for monitoring irregular or moving surfaces, e.g. in robots, pliable machinery, or as an artificial skin.

Integrated optical interconnections have the advantage that they are insensitive to electromagnetic interference, applicable in harsh environments, and highly sensitive. Last year, IMEC already reported embedded optical links on rigid surfaces. The current research takes optoelectronics one step further. Standard commercially available GaAs photo-detectors and GaAs vertical-cavity surface-emitting lasers (VCSELs) are thinned down to 30µm. Next, they are embedded into a flexible foil of optical transparent material and optically coupled with embedded waveguides and out-of-plane micromirrors. The resulting structure shows good adhesion and flexible behavior.

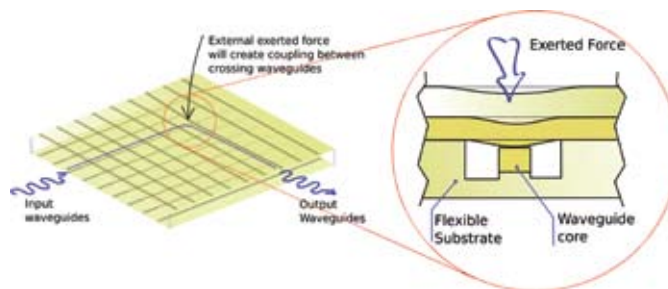
With this technology, IMEC is working on two types of sensors: array waveguide sensors and

optical fiber sensors. Both can be used for sensor foils. Array waveguide sensors rely on the change in coupling between arrays of crossing waveguides. Two layers of polymer waveguides are separated by a thin layer of soft silicone. When no pressure is applied, no crosstalk is detected. But when pressure is applied to the foil, the distance between the waveguides in the separated layers decreases, and light is transmitted from one layer to the other. This low-cost sensor is ideally suited for high-density pressure sensors on small areas.

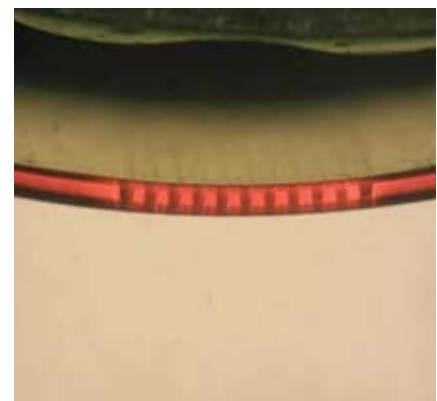
Optical sensing foils combine two technologies that have lately seen a growing interest: integrated optical interconnections, and flexible, stretchable electronics. The ambition of researchers is to create a flexible and stretchable skin-like foil sensitive to

touch, pressure, or deformation. Such artificial skin could be used in medical and industrial environments. To this aim, a group of European research institutes, including IMEC, are collaborating in the 7th Framework project PHOSFOS (Photonic Skins For Optical Sensing).

PHOSFOS will develop photonic foils based on optical fiber sensors. These foils are targeted at applications in civil engineering and medicine. They will, for example, continuously monitor the integrity and the behavior of buildings, dams, bridges, roads, or tunnels. Other uses are monitoring aircraft wings, helicopter blades, or windmill blades. They will enable early warning of failure or anomaly. Skin-like PHOSFOS membranes will also be used in long-term monitoring of respiration and cardiac activity, as well as the detection of pressure points under bed-ridden patients.



Principle of the array waveguide sensor.



Optical foil, bended with radius of curvature of 1 cm.

Patents

Europe

- Optical system with a dielectric subwavelength structure having a high reflectivity and polarisation selectivity. (EP 0 798 574)
- Floating body cell memory device and a method for the manufacturing thereof. (EP 1 693 898)
- Dielectric constant (k-value) enhancement of Hf comprising compositions. (EP 1 372 160)
- CMOS semiconductor devices with selectable gate thickness and methods for manufacturing such devices. (EP 1 315 200)
- Organic light-emitting device with field-effect enhanced mobility. (EP 1 808 911)
- Molecules suitable for binding to a metal layer for covalently immobilizing biomolecules. (EP 1 798 250)

Japan

- Megasonic cleaner and dryer system. (JP 4114188)
- A method for producing micromachined devices and devices obtained thereof. (JP 4128764)

USA

- A method for producing micromachined devices and devices obtained thereof. (US 7,347,557)
- Method for selective deposition of a thin self-assembled mono-layer. (US 7,368,377)
- Design method for RF MEMS devices and devices resulting therefrom. (US 7,372,346)
- Methods for bonding and devices according to such methods. (US 7,378,297)
- Method for extracting the distribution of charge stored in a semiconductor device. (US 7,388,785)

- Dry etching of poly Si gates doped with Yb. (US 7,390,708)
- Etching of structures with high topography. (US 7,393,768)
- Formation of deep airgap trenches and related applications. (US 7,396,732)
- Impurity measuring method for Ge substrates. (US 7,399,635)
- Formation of deep airgap trenches and related applications. (US 7,400,024)
- Electrostatic discharge protection device. (US 7,405,914)
- Megasonic cleaner and dryer system. (US 6,928,751)
- Megasonic cleaner and dryer. (US 7,100,304)
- Composition and method for treating a semiconductor substrate. (US 7,422,019)

Awards

- The paper entitled 'Creep behavior of mixed SAC 405/SnPb soldered assemblies in shear loading' won the **Best Paper Award** at the 9th Electronics Packaging Technology Conference (EPTC) 2007. Authors of the paper are **P. Limaye** (also at K.U.Leuven), R. Labie, B. Vandevelde, D. Vandepitte (K.U.Leuven) and B. Verlinden (K.U.Leuven).
- **Ybe Creten** received the **Best Young Scientist Award** at the annual International Workshop on Low Temperature Electronics (WOLTE) 2008 for her paper entitled 'Flash analog-to-digital converter operational in an ultra wide temperature range (room temperature to 4.2K) in standard CMOS technology'. Co-authors of the paper are P. Merken, R. Mertens, W. Sansen (K.U.Leuven) and C. Van Hoof.
- The paper entitled 'A prototype for practical eye-gaze corrected video chat on graphics hardware' won the **Best Paper Award** at the International Conference on Signal Processing and Multimedia Applications (SIGMAP), July 2008. Authors of the paper are M. Dumont (Hasselt University, Belgium), S. Maesen (Hasselt University), **S. Rogmans** (IMEC) and P. Bekaert (Hasselt University).
- For the second time, **IMEC** has **awarded students from several Faculties of Engineering in Flanders, Belgium**, who have contributed to the field of micro- and nanoelectronics through their thesis. For the academic year 2007-2008, IMEC granted the following students:
 - **F. Schoofs**, Catholic University Leuven (K.U.Leuven), for his thesis entitled 'Pd-H as actuator material' (supervisors: J. Fransaer and J. Van Humbeeck);
 - **S. Heyvaert**, Vrije Universiteit Brussel, for his thesis entitled 'Advanced coupling structures for waveguide based optical interconnection on printed circuit boards' (supervisors: H. Thienpont and C. Debaes);
 - **R. Stevens**, ETRO, Vrije Universiteit Brussel, for his thesis entitled 'Spatial, direction-adaptive transforms for scalable image decoding' (supervisor: A. Munteanu);
 - **T. Van den Hauwe**, ETRO, Vrije Universiteit Brussel, for his thesis entitled 'Design of the input stage of a 3D camera pixel' (supervisor: M. Kuijk);
 - **M. De Bock**, Ghent University, for his thesis entitled 'Design of a low power high speed sigma-delta modulator' (supervisor: P. Rombouts).

Events

2008 Software Defined Radio Technical Conference and Product Exposition

October 26-30, 2008,

Hyatt Regency Crystal City, Reagan Nat. Airport, Washington D.C., US

Reconfigurable radio technologies are moving into mainstream acceptance in a number of markets, reflecting the ability of these technologies to solve real problems in the wireless space. As a result, SDR 2.0, the next wave of innovation in both software-defined and cognitive radio technologies, will be driven more by market need than by technical vision.

During this SDR Forum, IMEC will demonstrate its SDR solutions for mobile terminals in one live wireless demo setup and complementary design methodology demonstrators. Main features that will be shown are flexibility in the RF transceiver and reprogrammability of the baseband platform together with the unique low-power and high-performance behavior of the SDR solution.

More information: www.sdrforum.org

Silane Safety Seminar

November 4-5, 2008, IMEC, Leuven, Belgium

Recently significant incidents occurred with the use of silane. Silane is an electronic specialty gas that has widespread use in the semiconductor fabrication industry. Since the mid 80's a series of silane technical and safety seminars were conducted in the US and Europe, creating the awareness of potential problems. These helped to drastically reduce the number of incidents and/or their severity. The last ten years, the LCD and PV manufacturers have expanded significantly; in 2008 they will use more silane than the IC companies. Recently, significant incidents occurred with the use of silane highlighting the need to conduct the seminars again.

Various suppliers are contributing to this one-day safety seminar which will bring together many acknowledged experts on silane, standards and regulations.

More information: www.ssaevents.org

IMEC Executive Seminar

November 11, 2008, Hotel New Otani, Tokyo, Japan

As IMEC's yearly event, the Executive Seminar brings industry executives and research managers together with senior IMEC research staff to discuss the upcoming technological challenges. The attendees will get a balanced and exclusive insight into the challenges and opportunities the industry will face during the coming years. Topics like (sub-)32nm CMOS scaling, 3D packaging, heterogeneous integration, wireless communication, biomedical electronics and the latest developments on efficient and renewable power will be covered.

More information in the events calendar on: www.imec.be

3D integration workshop

A unique forum to debate on 3D integration issues, technological options, standards & conventions and roadmaps

November 13-14, 2008, Hsinchu, Taiwan

IC manufacturers and research groups are scrambling for a part of the 3D integration action. The first appliances with 3D chips are already available, with many more to come. But there are still a lot of questions surrounding 3D. Will 3D be limited to niche applications or will it become a widespread technology? Will 3D be cost-effective? What is the roadmap for 3D, and which of the many technical options will be used? How can 3D systems be tested? What are the requirements for the supply chain?



The aim of this 3D integration workshop is to discuss different views and initiate and stimulate the route towards standardizations in 3D.

- **Who should attend?** The whole 3D supply chain: IC manufacturers, the fabless community, tools and equipment suppliers, material suppliers, packaging and test houses and EDA suppliers.
- **Format:** Each session will start with a presentation of the consolidated view of major 3D players on key 3D technology topics, followed by an interactive discussion.
- **Organized by IMEC and IMEC Taiwan.**

More information: www.imec.be/3Dworkshop

PESM 2009

2nd International workshop on Plasma Etch and Strip in Microelectronics

February 26-27, 2009, Novotel, Leuven, Belgium

Continuing downscaling of semiconductor devices brings new challenges for plasma etch and strip. New materials (high-k and low-k dielectrics, metal gates, phase-shift memories etc.) and new architectures (3D devices, channel-engineered devices etc.) require new etch and strip approaches. IMEC organizes this workshop to bring together people from research institutions and industry to discuss new challenges in plasma etch and strip.

More information: www.pesm2009.be

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ARRM 2009 – IMEC Annual Research Review Meeting 2009

June 3-4, 2009, Hotel Crowne Plaza, Brussels, Belgium

Celebration
edition

Next year's IMEC Annual Research Review Meeting will take place in June and will be organized in the frame of IMEC's 25th anniversary. On the first day, prominent speakers from the semiconductor industry worldwide will focus on the future strategy for scaling and non-scaling activities, on the changes in business approach and collaboration opportunities with R&D centers. Additionally, you can attend panel discussions on biomedical electronics and photovoltaics. On the second day, you will be part of the IMEC Research Business Forum. Don't miss this celebration edition.

More information soon in the events calendar on www.imec.be



IMEC IS GOING GREEN. YOU TOO?

Please subscribe to the electronic newsletter on www.imec.be/subscribe-newsletter

