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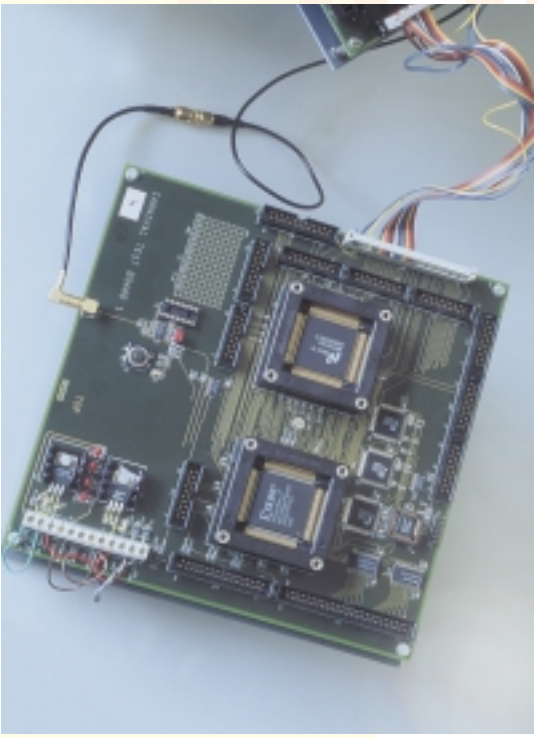
Annual Research Review Meeting 2000

5GHz Wireless OFDM modem reaching data rates up to 54Mbit/s

The wireless modem was built around IMEC's OFDM baseband ASIC. This test setup resulted in the world's first demonstration of wireless OFDM communication in the 5GHz band at such high data rates.

Applications like Internet and in-home entertainment together with the increasing interest for personal services on portable devices that are always on and always connected, stimulate the demand for low-cost broadband wireless networks.



Test board for wireless OFDM point-to-point communication

To realize seamless proliferation of these multimedia services in the home, IMEC is developing the next generation of broadband wireless local area networks (WLAN). The goal is to achieve a wireless communication between two or more terminals, with a capacity of well over 100Mbit/s, based on orthogonal frequency division multiplexing (OFDM) communication.

At last years annual research review meeting, IMEC presented its first baseband ASIC, designed in 0.35µm CMOS technology. This application specific processor integrates the entire OFDM functionality and is in line with emerging standards for

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New IIAP on advanced flash memory concepts

IMEC launches industrial affiliation program (IIAP) on flash memory technology.

This new program concentrates specifically on integration issues for embedded flash modules in CMOS. Besides IMEC's activities on its own proprietary flash technology (registered as HIMOS® in Europe and the US), this IIAP mainly concentrates on more generic topics that are of mutual interest for most flash cell concepts. To provide sufficient leverage also towards other flash cells and technologies, the program is not directly linked to IMEC's HIMOS® technology development program. Based on IMEC's extensive know-how on flash memory (presently 0.18µm HIMOS®), it was decided to establish a new R&D program with emphasis on the 3 following generic platforms: scaling, reliability and advanced concepts. The scaling platform comprises basic non-volatile memory device physics for the 0.13µm generation and below,

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From microelectronics to nanoelectronics

As the shrinking of CMOS circuits is now approaching the critical scale of 100nm, there is a strongly increasing interest for the possible use of nanoelectronics for future development of IC technology. For example, the latest revision of the international technology roadmap for semiconductors (ITRS) will include for the first time a survey of alternative device technologies, which could complement CMOS development or extend the scaling process beyond the CMOS limits as they are currently perceived.

In the past, IMEC has built considerable expertise in the most important quantum well (QW) device technologies (high electron mobility transistor, heterojunction bipolar transistor, QW laser). This background is now exploited in various (mainly telecom-oriented) application projects. IMEC has also actively participated in the research on the so-called "second generation devices", specifically vertical heterojunction MOS, single electron memories and spin valves. The early phase of this activity was mainly funded by European Union programs (ESPRIT Long Term Research). Today, development is continuing towards integration of these devices into functional circuits, both for logic and non-volatile memory applications. At the same time, the latest generation of nanoelectronics, mainly based on molecular technology, is now under investigation for applications in the biosensor and bio-actuator area. On the European scene, networking activities constitute an important complement to the technology development projects. For many years, IMEC occupied a leading position in nanoelectronics networking through the PHANTOMS NoE. Today, the NEON network and the EURACCESS project provide new opportunities for collaboration in a European context. At the regional level, IMEC is coordinating a Flemish interuniversity nanotechnology research consortium around the use of its new electron beam writer.

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broadband multimedia indoor communication in the 5GHz band such as ETSI Hiperlan/2, IEEE802.11a and MMAC. During the past year, the ASIC has been fully evaluated. Meanwhile, the system was extended with a discrete RF front-end, operating in the 5GHz band. With this test setup, the first-of-its-kind wireless OFDM point-to-point communication in the 5GHz band was demonstrated. As OFDM is a new modulation scheme, most of the performance results are based on simulation data. With the prototype system at hand, the knowledge of the practical performance of OFDM for broadband wireless communication will be expanded.

Currently, integration of the baseband processor together with the RF front-end in a single package is targeted. For this purpose, IMEC's MCM-D (thin-film multi-chip-module) technology was used. This single-package integration will enable the realization of high-performant, low-cost and low-power wireless communication systems.

In parallel, an improved OFDM baseband ASIC has been developed in a 0.18µm CMOS technology. A more complex modulation technique (64 quadrature amplitude modulation) was used to achieve data rates of up to 54Mbit/s. This ASIC will be the cornerstone for a wireless network, consisting of several base stations and mobile terminals, with a network capacity exceeding 100Mbit/s.

Low-cost infrared detector arrays

IMEC developed linear arrays of uncooled polySiGe microbolometers and linear InGaAs arrays for NIR (near infrared) spectroscopy or imaging applications.

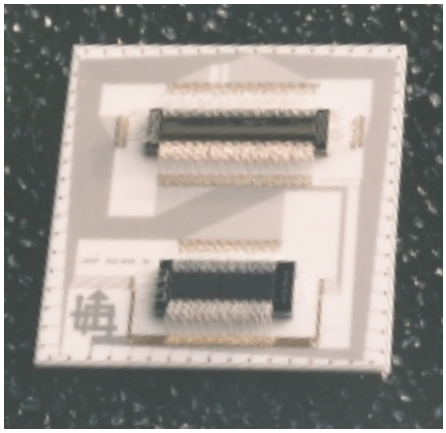
Low-cost uncooled thermal infrared detectors are expected to open a wide variety of commercial applications in the near future, e.g. enhanced night vision in automotive & security systems and intelligent industrial & medical monitoring. Only uncooled thermal detectors, fabricated using CMOS technology, can achieve the necessary low-cost for mass-market application.

Extended-wavelength InGaAs linear detector array

IMEC developed linear arrays of uncooled microbolometers, using polySiGe as resistive detector material. To this end, new surface-micromachining process steps were developed such as vapor HF release, the use of U profiles for structural stiffness enhancement, and TaN infrared absorbers. Combined with CMOS fabrication technology, microbolometers with extremely high thermal insulation levels (below 10^{-7}W/K), and superior uniformity and yield could be realized. First results indicate a noise equivalent temperature difference below 100mK. To realize future 2-dimensional microbolometer cameras, different detector/-read-out integration schemes are under development.

IMEC also developed linear InGaAs arrays for NIR spectroscopy or imaging applications such as on-line process monitoring in the (petro)chemical industry, moisture measurements on tobacco, sugars, and other powders in food industry, identification in cosmetics and pharmaceutics, and telecom applications.

The need for significant cost reductions in the infrared-imaging world drives research on epitaxial growth and processing of NIR arrays on large inexpensive substrates. At present, only GaAs is a suitable candidate for low-cost infrared detectors, especially because large 6” substrates are readily available.



MCM hybrid of microbolometer array and sensor readout ASIC

IMEC has developed NIR InGaAs material that shows characteristics close to the theoretical (bulk leakage) limits and the improvement by cooling is not defect limited. From this material, 128 pixel line-arrays were realized. The arrays will be cooled to –25°C using two-stage Peltier coolers. Currently, 2-dimensional NIR cameras are under development, using flip-chip indium-bump technology, together with different detector/read-out integration schemes.

Infrared-imaging components based on IMEC's technology will be commercially available through XenICs, a new IMEC spin-off.

Platform-based design of reconfigurable Internet appliances with OCAPI-xl

IMEC has developed a C++ library for system design of mixed hardware/software architectures, called OCAPI-xl. It uses a unified model to represent both hardware and software, allowing a fast exploration of the hardware/software partitioning. The model is executable and can be refined to hardware and software. These features make OCAPI-xl a good choice for the design of reconfigurable appliances.

Designs like an Internet protocol stack have their implementation targets evolving in time (e.g. from workstations to micro-controller or dedicated hardware implementations). So have the system descriptions to express the protocol-stack functions. Each time a new platform is aimed, the same black magic is needed to port the specification from one target to another. A possible approach to solve this problem is OCAPI-xl, which supports the creation of a target-independent system specification, even beyond the decision for hardware or software implementation.

OCAPI-xl provides a unified model-

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System design challenges in the post-PC era

In his keynote speech at this year's Design Automation Conference, Professor Hugo De Man, senior research fellow at IMEC and professor at the Katholieke Universiteit Leuven, presented major system design challenges posed by the post-PC era.

Progress of microelectronics, DSP, integrated sensors and RF CMOS causes a paradigm shift in the ICT world referred to as the "post-PC" era when wearable computing augments our consciousness, protects our health and globally connects people and things. Designing such systems differs radically from designing CPU architectures.

Until recently, chip developers were designing standalone ASICs, processors, and other complex ICs. System experts built systems by interconnecting different chips on a PCB. Emerging deep submicron process technologies enable the integration of dozens of processors onto a single chip. Hardware as well as software IPs can be integrated to create a system. By entering the post-PC era, designers can no longer think in terms of hardware description languages such as Verilog and VHDL. Yet, SoC design demands for designers with hardware, software and system knowledge.

As CMOS technology is further scaled down, process costs (such as mask cost) are rapidly increasing. It is expected that from 100nm on, costs will be too high and development time too long for customized ICs. "There will be an increasing tendency towards the design of reconfigurable hardware platforms for series of applications instead of traditional chip design," says Hugo De Man. "Design methodologies will shift from EDA (electronic design automation) to the implementation of intelligence in systems, so that a general hardware platform can be easily progammed for dedicated applications."

The art will be to design a diversity of cheap, energy efficient, yet programmable platforms that can be configured over the Internet and communicate with humans through non-keyboard interfaces. It requires a grand convergence of previously separated domains such as programmable/reconfigurable multi-processor architectures with embedded software, broadband radio, MEMS (micro-electromechanical systems) and biosensor interfaces. Designing these platforms goes far beyond the capabilities of today. Up to now, EDA industry concentrated on efficient design of mainly digital ASICs. Current EDA tools do not even offer systematic design of both hardware and embedded software. Tool vendors will have to concentrate on developing architectural level design tools, which are very difficult to create. Not only hardware and software knowledge is required. System design expertise addressing new fields like biology, sensors and mechanics, … forms a vital link. Only multi-disciplinary teams can cover this broad range of expertise necessary to solve the architectural design problems.

"Electronics industry will have to invest in wide-ranging research to create a standardized architectural methodology. Only the right mix of people in areas of expertise can tackle this challenge successfully," concludes Hugo De Man.

ing style in C++ to represent both hardware and software parts of a system. Switching a process from hardware to software implementation or vice versa does not require a code rewrite. It also provides a system model that expresses parallelism and introduces a common notion of time between the hardware and the software processes at different levels of abstraction. In addition, a set of high-level communication primitives are introduced, which allow to describe a wide range of applications and which can be refined to both hardware and software. Finally, it offers a refinement method and code generation to multiple targets: hardware (VHDL, Verilog) as well as software (C processes on OS).

The OCAPI-xl modeling style can describe mixed data and control flow systems, making it a very suitable environment to design Internet appliances. Since the unified model is implementation independent, it can be mapped quickly on different implementation platforms depending on the appliance.

The Go4Net reconfigurable Internet appliance is the first demonstrator built using OCAPI-xl. It runs a GIF encoder application that can be remotely reconfigured and connected to a camera. This implementation is a full hardware FPGA solution. It consumes 700mW (2W with the sensor) and can achieve a throughput of 80Mbit/s. As a next step, the same high-level model will be mapped on an embedded processor to demonstrate the platform independence.

Further research focuses on protocols to ensure the robustness of the reconfiguration and dynamic reconfiguration. In addition a technology-independent FPGA configuration will be developed, allowing the mapping of a single configuration stream on a wide span of FPGAs.

IMEC supports SmartMove's efforts to standardize digital short range communication

SmartMove investigates IMEC's OFDM (orthogonal frequency division multiplexing) technology as base for digital short-range communication

SmartMove is an IMEC spin-off with nearly 100 employees. It develops an open telematics platform for vehicle communication. Vehicle telematics combines advanced computing power with telecommunication and positioning systems such that an unlimited number of services can be offered to the driver and passengers. The SmartMove platform is a so-called third generation system. It can implement already existing systems and integrate them in one single system. It is an open system, based on Java technology that enables new applications through one standard platform. Several communication channels are combined, such as GSM, DSRC, TCP/IP,…

DSRC enables data transmission between a beacon and the mobile platform within a distance of 100m. Numerous applications are possible such as downloading multimedia images in the car (e.g. road maps, movies, …), electronic toll collection, parking information, local (city) information and safety enhancement (e.g. electronic transmission of road information, traffic density, …).

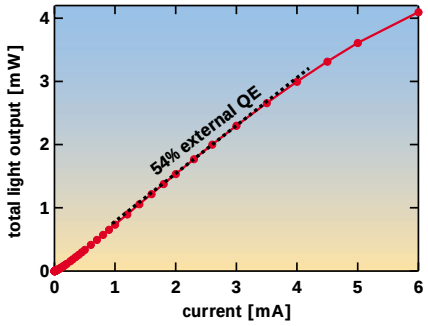
SmartMove is an active member of the US standardization committee "DSRC standards writing group", set up by US DOT (Department of Transportation). This group is currently standardizing DSRC. For this purpose, SmartMove has set up a research project with IMEC to use IMEC's OFDM technology as base for DSRC. DSRC applications require high bit rates combined with high reliability that can be realized with OFDM. OFDM systems adapted towards DSRC realize potential data rates of 24Mbit/s. Moreover, OFDM can manage multi-path signals very efficiently, such that it is very suited in the harsh and highly dynamic environment of 'fast moving metal' that the roadside is. Note that the current band set aside for DSRC is in the 5.8 GHz range, which complicates issues like reflection, doppler shifts and multi-path even more. OFDM is also very useful to eliminate frequencies that are disturbed by strong interference, which is essential for vehicle communications. Furthermore, it also offers the potential advantage that it will become possible to connect the car to the in-home or in-office wireless network when entering the garage. Getting information from the 'local city loop' is also a possibility.

In a second phase of the project, the required modifications to IMEC's OFDM modem chip will be investigated to make the chip useful for DSRC. Based on these results, a possible new ASIC will be designed that can be used in different operating modes such as direct communication of the vehicle with the in-home network, communication with road beacons, …

54% Efficiency LEDs

In collaboration with the Vrije Universiteit Brussel and the University of Erlangen, Germany, IMEC has developed high-efficiency surface-textured light-emitting diodes (LEDs), suitable for integration into one- or two-dimensional arrays.

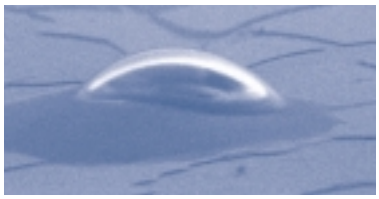
In conventional LEDs, total internal reflection of light at the semiconductor-air interface limits the efficiency to 2%. This problem can be overcome by a non-resonant cavity (NRC) LED design, which comprises surface texturing and the application of a rear reflector on a thin-film LED. The light extraction is significantly increased, thanks to light scattering at the textured surface.



Output power versus current of an encapsulated NRC-LED

IMEC's NRC-LEDs emit at a wavelength of 860nm. The LED diameter, before encapsulation, is 45 microns. The LEDs can be encapsulated on a wafer by means of a dome of transparent epoxy on top of the LED. The required current to emit 2mW of light is merely 2.6mA. This corresponds to an absolute external quantum efficiency of 54%, which is only slightly less than the world record of 55%. Moreover, more than 4mW of light is emitted with only 6mA.

The LEDs are useful for applications where a high surface-emitted intensity is required, or for communication applications that demand an array of small, yet intense light sources.



SEM photograph of an NRC-LED encapsulated on a wafer

Hybrid integration of thinned metamorphic HEMTs on germanium

IMEC developed a highly selective technique for substrate removal, which is very convenient to integrate Ge MHEMTS in low-cost MCM-D substrates. Combined with the low environmental load of this method, the process provides a high-performance technology ready for advanced hybrid integration.

Research in monolithic microwave integrated circuits (MMIC) is driven by a growing demand for low-cost, high frequency microwave systems in application fields such as the automotive industry.

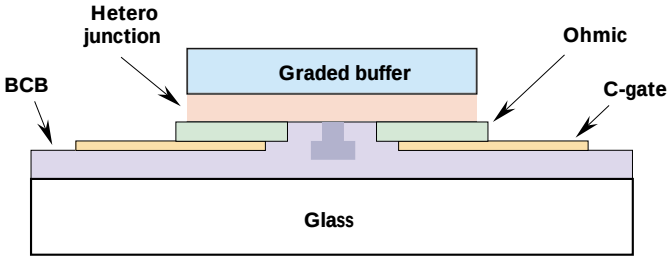
An important step in this direction is the successful hybrid integration of thinned metamorphic high electron mobility transistors (MHEMTs) on germanium (Ge) in IMEC's thin-film multi-chip-module (MCM-D) technology. Integration of thinned individual HEMTs with passive circuitry on these MCM-D substrates can result in low-cost advanced hybrid systems for mass-market millimeter wave applications.

High-performant InGaAs/InAlAs MHEMTs can be fabricated on low-cost Ge substrates. However, Ge has a limited resistivity, introducing large parasitic capacitances and resistances, which dramatically reduce the high-frequency performance compared to GaAs substrates. Removal of the conductive substrate is the most feasible solution for this problem.

The diced chip is mounted on a glass substrate (MCM-D), active side of the chip facing the glass, in a 3µm thick polymer layer (BCB). The frontside of the chip is now protected by the BCB. The Ge substrate can be removed by RIE (reactive ion etching). Main advantage of this plasma method is the high selectivity of Ge towards GaAs, which is the first epitaxial layer on top of the substrate.

The GaAs buffer can then be removed selectively in a sulfuric acid based solution. As a final processing step, the metamorphic transition buffer, used to transform the

lattice constant of the Ge substrate into the one of InGaAs/InAlAs, needs to be removed outside the active region. Therefore, a lithography step has to be performed and a non-selective etching, based on phosphoric acid, is used. After this step, the metal contacts of these very thin devices (2µm) are revealed and can be contacted by probe needles from the backside. To be able to integrate these transistors in MCM-D substrates, their thickness has to be less than 5µm to circumvent planarization problems in subsequent MCM-D processing steps. Substrate removal also serves to solve this problem.



Cross section and photograph of a thinned MHEMT glued in a BCB layer on glass

Measurements done on these glass (MCM-D) wafers reveal a slightly reduced DC performance compared to devices based on GaAs substrates, but the RF performance recovers and is almost as good, reaching an f_T of 70 GHz.

Technology report

Simulation of quantum leakage currents in MOS inversion layers using nuclear decay theory

The reduction of the deposition temperature of poly-SiGe and the increase of maximum post-processing temperature on CMOS wafers allow post-processing of MEMS on standard CMOS wafers.

Recently the ESPRIT project QUCUISS was finalized. This project was devoted to the physical modeling of leakage currents in inversion layers, caused by quantum mechanical tunneling through ultra-thin dielectric layers. The topic is of great interest for downscaling CMOS since gate leakage currents are an important design issue e.g. for portable applications.

Although quantum leakage currents have been modeled for some time, a complete understanding that is fully in agreement with the rules of the quantum world was still lacking. In the QUCUISS project this issue has been addressed and a model of quantum currents has been derived based on analogy with nuclear decay. Just as an unstable nucleus may decay, an electron in an inversion layer may reside in a subband state for a limited time. Therefore, an essential ingredient in the expression for the quantum-leakage current is the lifetime of electrons in such states. The nuclear-decay theory, developed in the thirties by the famous physicists Gordon Breit and Eugene Wigner, was exploited in this project. The theory has been adapted for the behavior of electrons in an inversion layer. Whereas a nucleus can only decay once, a subband can be refilled and participate again in the current generation. A good agreement was achieved between the theory and experimental data obtained by STMicroelectronics and IMEC. Furthermore, the results were compared with the predictions from the models for quantum-leakage currents that were derived by researchers from ETH using Bardeen's perturbative methods. Again good agreement was obtained. These results enhance our confidence in the theoretical modeling of quantum leakage currents. The software has been integrated in the ISE tool suite. (Funding from the EC is gratefully acknowledged.)

Technology report

Low-noise particle detector front-end ASIC for space missions

IMEC designed a programmable, mixed analog-digital, low-noise particle detector front-end ASIC intended for various space experiments.

The increasing demand to lower the cost of space missions is a driving force to reduce size and power of space instrumentation. That's why ESA is developing a chipset for particle detection front-end and back-end electronics. The back-end is based on an 8052 microcontroller and both masters the system and takes care of the data generated by the particle detector front-end (PDFE) ASIC. The low-noise, low-power PDFE was designed by IMEC in a standard 0.7µm process. The chip comprises besides the analog amplification chain an 8-bit analog-to-digital converter and control logic.

The analog chain consists of a charge-sensitive amplifier, which integrates detected particles, and a pulse-shaping amplifier, which shapes the signal into a semi-gaussian pulse to increase the signal-to-noise ratio of the chain. The amplitude of the pulse is a measure for the energy of the detected particles. A baseline restorer is integrated in the analog chain to eliminate the effect of random offset on the DC level of the shaper output. The analog chain also comprises a peak detector that holds the maximum value of the semi-gaussian pulse during conversion by the ADC, and a discriminator that detects the occurance of an event. The ADC runs at 250kHz and is a subranging two-step flash structure. A second analog channel is provided for (anti-) coincidence purposes.

The ASIC is made as versatile as possible by implementing several digitally programmable operating modes. These modes can be selected through a serial link. Through this link, several ASICs can be cascaded, allowing easy scalability and hence further enabling the use of the PDFE in various instruments.

Layout of the analog port of the PDFE ASIC

The total equivalent noise charge of the chip is 800 electrons rms at 100pF detector capacitance, 1nA detector leakage and a shaping time of 1µs. The conversion gain is 30mV/fC and the maximum detectable charge is 0.1pC. The fully operational chip consumes only 50mW power. A baseline shift of 15mV is realized at a maximum counting rate of 250kHz for inputs limited to 2.5fC (25kHz for 0.1pC). To make the chip as insensitive as possible for radiation (single-event upset and total dose radiation), special design techniques were used both at the transistor and architectural level.

Industry link

Philips and IMEC fully cooperate on 100nm CMOS development

Philips and IMEC have entered into a strategic alliance to accelerate the development of 100nm CMOS, which requires merging of high-level capabilities.

The enormous technological challenges in next generation IC technologies and the increasing market pressure force partnerships between companies and R&D centers such as IMEC. The joint research project IMEC-Philips strengthens their worldwide position in state-of-the-art silicon technologies.

IMEC and Philips already worked together on 100nm CMOS development within the IST project HUNT (HUndred Nanometer CMOS Technology). The strategic alliance between Philips and IMEC is strongly linked to the activities in HUNT, but goes much beyond this.

The main target of the cooperation is to develop a 100nm CMOS technology based on a scaled-down version of planar CMOS technology such as 130nm. Both process steps and modules will be pushed to their limits. In parallel, possible alternatives will be investigated as back-up solution, which will also be implemented for the 70nm node and below. The joint development will cover all process steps: lithography, etching, cleaning, new materials for both low-k and high-k dielectrics and Cu deposition.

Shallow-trench isolation, gate stack, ultra-shallow junctions, silicides and back-end Cu/low-k modules will be integrated into a full process. The results obtained in IMEC's industrial affiliation programs (IIAPs) on 193nm lithography, cleaning, silicides, low-k and Cu damascene will be exploited for this 100nm CMOS development.

"Both Philips and IMEC are internationally renowned institutes, which can accelerate their innovation by international collaboration projects," says Gilbert Declerck, President and CEO of IMEC. "After 6 months, the cooperation between IMEC and Philips has already resulted in an acceleration in the research on 100nm CMOS." As such, 100nm CMOS will be introduced much faster than expected.

"By creating a larger pool of brainpower, IMEC and Philips can take advantage of their respective strengths," states Max Collet, Senior Vice President of Philips Research. A complete 100nm CMOS process will be developed and integrated at IMEC premises with focus on applications.

IMEC's high-k industrial affiliation program gains momentum through partnership with International SEMATECH

IMEC has a long-standing expertise in growth, characterization, reliability and process integration of thin gate dielectrics. This background provides a solid base for its current industrial affiliation program (IIAP) on high-k dielectrics. The recent partnership with International SEMATECH, with its expertise in materials screening and techniques, tool/process evaluation and tool manufacturing worthiness development, rendered this program a rocket start in finding a suitable material for future gate stack technology.

IMEC's IIAP on high-k dielectrics targets the development of manufacturable processes for the gate stack needed for sub-100nm devices with low leakage current and high reliability. The IIAP covers all required aspects to develop this new gate stack: deposition of high-k dielectrics using ALCVD (atomic-layer chemical vapor deposition) and MOCVD (metal-organic CVD), cleaning and contamination control, physical and electrical characterization of high-k materials, reliability of gate stack and transistors, metal gates, process integration issues and ES&H (environment, safety and health) considerations.

As semiconductor devices are further scaled down, traditional processes and materials reach their physical limits. Thinner effective gate dielectrics for sub-70nm devices have to be used. "Silicon dioxide, which has been the heart of the MOS transistor for over 40 years, now has to be replaced," states Marc Heyns, director of IMEC's high-k program. "This enormous technological challenge requires a global collaboration to meet the requirements of the international technology roadmap for semiconductors (ITRS)."

Considering these huge problems, it is extremely important to coordinate these new gate stack activities on a global scale. By sharing cost and risk in a global project, and by combining expertise, one of the major roadblocks of the ITRS can be overcome. IMEC has a long-standing relationship with several member companies of International SEMATECH who were aware of IMEC's potential and thus favored the idea of forging a link between their respective high-k programs. International SEMATECH is the first to cooperate in IMEC's advanced gate stack program. "The collaboration with International SEMATECH brings together a majority of the world's semiconductor manufacturers," says Gilbert Declerck, President and CEO of IMEC.

"Non-SEMATECH members are also invited to join the program, so that a worldwide collaboration and consensus for these new gate stacks can be achieved."

International SEMATECH and IMEC will work together to develop effective equipment, materials and processes for gate stacks for 100nm and smaller semiconductor devices. This will include, among other activities, evaluation of various high-k dielectric materials; development of processes for depositing those materials; evaluation of various metal stacks, development of cluster integrated processes; fabrication of etched gate structures and feasibility study of potential integration in full CMOS processes. The initial EOT (effective oxide thickness) targeted is 1nm. However, the final aim is a feasibility demonstration of 0.5nm EOT gate stack. Both organizations will add their specific

strengths to the joint program. IMEC has world-class skills and talent in major areas relevant to the project, such as surface conditioning and cleaning, physical and electrical characterization of dielectrics and device reliability studies. IMEC's pilot line offers the possibility of performing full-process compatibility studies of the novel materials and techniques.

International SEMATECH is a non-profit research and development consortium of the following semiconductor manufacturers: AMD, Conexant, Hewlett-Packard, Hyundai, Infineon Technologies, Intel, IBM, Lucent Technologies, Motorola, Philips, STMicroelectronics, TSMC, and Texas Instruments. Additional information on International SEMATECH can be found at http://www.sematech.org.

XenICs, a new IMEC spin-off, launches onto the infrared spectroscopy and imaging market

IMEC's latest spin-off company XenICs NV develops and markets new infrared image sensors. These image sensors are based on a number of patented technologies and on key know-how which, in exchange for a shareholding, IMEC has brought to the new company via exclusive license agreements.

XenICs
Partnering Your Infrared Solution

The next century will see a revolution in the infrared imaging and spectroscopy market with a shift to uncooled and cheap devices. The potential applications of these devices are enormous, provided that system prices will be drastically reduced. It is XenICs' vision that in the future infrared cameras will be available for 1.000 Euro or less such that they are affordable for any application.

Sales of infrared imaging devices have long been determined by high costs due to their cryogenic cooling requirements and their complex production processes. XenICs will license two innovating technologies from IMEC. One technology is based on new III-V semiconductor materials for infrared detection in the wavelength range from 1 to 5µm, the second is based on polySiGe micro-bolometers operating in the wavelength range from 8 to 12µm. Both technologies have the advantage that they require less to no cooling. They allow volume production on large substrates such that economies of scale become a reality. Other advantages include low power consumption, small pixel size, and the possibility of integrating a number of electronic functions together with the sensor on-chip.

Applications for infrared spectroscopy and imaging systems can be found in most industries for on-line quality control, process monitoring or for predictive maintenance. In addition, these vision systems can be applied in the automotive industry for improved night vision or improved vision in bad weather conditions. Other application domains are telecommunications, security for nighttime surveillance, medical applications, etc. At start-up, XenICs will mainly focus on sensor products, the heart of any infrared imaging system. These products will in general be sold to OEMs or system integrators that implement these components into their spectrometers, line-scan

cameras or 2D cameras. XenICs will address the market by focusing on the development of a range of standard products in order to keep costs down.

The new company also intends to collaborate with IMEC on the development of infrared image sensors for space applications, mainly for ESA (European Space Agency). XenICs already got support from the ESA Technology Transfer Program that stimulates the start-up of new spin-off companies that will make space technology available for civil use.

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New 157nm program attracts major semiconductor players

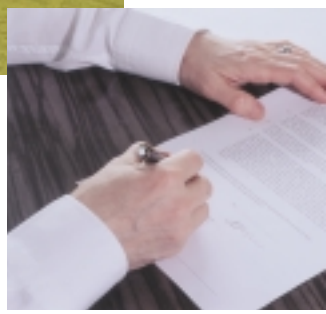
Shortly after IMEC's announcement of its new 157nm lithography process development program, several leading-edge semiconductor companies decided to join the program. This wide industrial collaboration aims to deliver manufacturable 157nm lithography processes by 2003.

Recently, 157nm lithography has become the most likely candidate for the critical layers of the 70nm node. It is clear that 157nm photoresist and process development, together with appropriate resolution enhancement techniques, will have to be completed within an accelerated time frame to meet the international technology roadmap for semiconductors (ITRS). Today, one of the major potential showstoppers is the timely availability of 157nm photoresists.

Last July, IMEC announced its 157nm lithography process development program aimed at delivering manufacturable 157nm lithography processes by 2003. The program is set up in close collaboration with ASML, who is currently developing a 157nm exposure system in an industry-wide 157nm lithography technology program.

The 157nm process development program focuses on (i) accelerating the development of appropriate resist processes and (ii) comparing the printing performance of 157nm reticles manufactured in different ways. IMEC is currently building the necessary infrastructure for a 157nm lithography cell, including a mid-field stepper, interfaced to a TEL track and with the necessary metrology equipment. The lithography cell will become operational mid 2001. The stepper has an NA up to 0.75 and uses a reticle magnification of 6, which closely approaches that of first generation full-field step-and-scan systems. This lithography cell allows resist companies and mask shops with an active 157nm development program, to have early access to such an exposure tool to test their own materials. Also IC manufacturers will be able to build up early experience with 157nm lithography for early dry etch and device development work.

In the meanwhile, TEL (Tokyo Electron Limited) has decided to join the 157nm program. The collaboration between IMEC and TEL will concentrate on resist coating thickness and CD uniformity optimization, and on the need for critical ambient control during coating and development of photoresist. TEL will provide its famous Clean Track ACT8 platform to be interfaced to the mid-field stepper, and metrology systems needed to develop a production worthy lithography cell.



Also nine leading-edge semiconductor manufacturers (including Advanced Micro Device, Infineon, Intel, Micron, Motorola, Philips, STMicroelectronics) are in the process of joining IMEC's 157nm process development program (status September 22, 2000).

The first ASML 157nm full-field scanner will be installed at IMEC to which the developed process will be transferred. At that time, a full-field scanner 157nm development program will be started, very similar to the current 193nm program, focusing on the 70nm and exploring the 50nm technology node.

continued from p.1

with a clear focus on tunnel and inter-poly dielectric scaling limitations as well as on alternative program/erase mechanisms. Secondly, the reliability platform addresses the main problems associated with endurance, retention, soft-write, disturb effects and stress-induced leakage currents, all of which are expected to become more and more critical with device scaling. The last topic deals with advanced or 'beyond-conventional' flash concepts that can boost the performance and scalability of tomorrow's non-volatile memories, such as dual-bit and multilevel schemes, and nano-flash cells using crested barriers for low-voltage tunneling.

Advanced device integration program

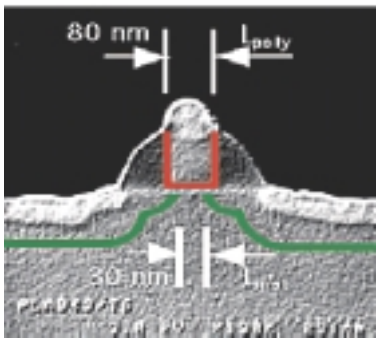
Increasing CMOS device performance for the 70nm regime and below is becoming increasingly more complex as compared to previous technology generations. Therefore, innovative solutions and breakthroughs with new materials and/or device architectures are required.

The objective of the Advanced Device Integration Program (ADIP) for sub-70nm technology is to experimentally identify the most critical limitations of scaling conventional CMOS while also investigating potential advanced or alternative solutions for further improvements of silicon based MOSFET technology.

CMOS experiments will focus on the front-end-of-line (FEOL) issues such as isolation, gate stack, channel doping, shallow junction and spacer technology and silicidation. The second component explores introduction of new materials and architectures such as SiGe, high k, double gate SOI, ….

The program also includes the support of advanced numerical and analytical simulation tools (quantum effects, …) and advanced characterization techniques (2D profiling, …).

The program provides a unique platform to prove and incorporate the advanced IMEC work on process steps into real devices.



Technology report

Radiation tolerant 180nm CMOS library

ASICs for space applications require radiation hard technologies. Two years ago, IMEC studied in an ESA (European Space Agency) project design methods to minimize total dose effects, and to circumvent single-event type radiation effects, such as single-event upset and single-event latch-up for VLSI standard cell libraries. Based on two studies, IMEC has developed for ESA a radiation tolerant cell library for the UMC 180nm CMOS technology. The library is expected to be single-event upset immune and total dose tolerant up to over 1 MRAD. Special techniques were applied to avoid leakage currents within the transistors and inter-device leakage, which are the major problems with total dose radiation. Using a deep-submicron technology is very beneficial for total dose performance, since as technologies are scaled, thinner oxides are used, resulting in an almost negligible shift in threshold voltage after radiation. Redundancy was used to avoid single-event upset. Compared to the commercial library, the gate density is only a factor two/three smaller. Validation of first silicon is being started. The European space industry shows great interest to use such a technology, since today's lack of radiation tolerant technologies in Europe is a major bottleneck in designing ASICs for space applications.

Silicon processing for ULSI circuit fabrication

The course offers a comprehensive, state-of-the-art, training program in the practice, fundamentals, and emerging trends of silicon wafer processing for deep submicron devices. It is useful for both professionals new to the semiconductor industry and for experienced engineers in the field that may not find adequate time to keep up with the rapidly changing technologies.

Who should attend: Engineers, supervisors, managers, and directors working in, or having responsibility for process development, field process support, process integration, device design, chip manufacturing, process and metrology tool development and support, materials for IC processing, and technical marketing and sales.

Scheduled on: October 23-26, 2000 at IMEC

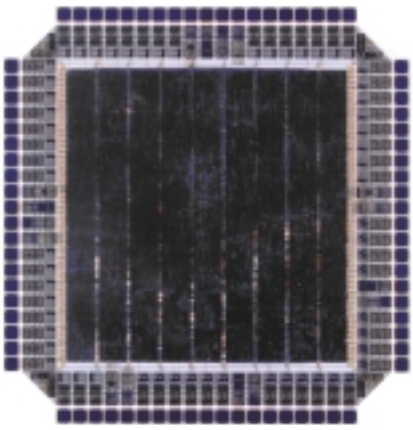
How to write code for high-performance low-power multimedia applications?

The course will focus on reduced cost, low-power-oriented system-level design approaches for the efficient realization of data-dominated applications, especially in real-time multimedia and telecom processing. The main emphasis will be on tradeoffs with respect to total system power and chip size or board size for given timing constraints. Data transfer and storage analysis techniques will be discussed, resulting in systems with higher performance and a gain of a factor 20 in power consumption. The approach is applicable both to hardware and software realizations. This course will be followed by a course on address optimization.

Scheduled at IMEC on: December 11-14, 2000
May 7-10, 2001
September 17-20, 2001
December 10-13, 2001

Layout training

Based on the success of a first program organized for Alcatel Microelectronics, MTC has set up in cooperation with the local employment office (VDAB) a second training program to retrain candidates without any knowledge of electronics to do layout. The program consists of three parts: a basic education in electronics by the local employment office, elementary knowledge in technology and layout, and practical training in layout. After this 5-week course, all 11 candidates will be able to draw a layout from a given schematic with a commercial EDA tool.



IMEC offers deep submicron layout service

IMEC offers a deep submicron layout service, starting from gate-level netlist. Over a period of 3 years, tens of circuits have been successfully taped out, for 3 up to 6 metal-layer processes, both for in-house developed systems-on-a-chip, as for ASICs developed by third party design houses, research institutes and universities. Circuit complexities handled were up to 500.000 equivalent gates, system clock-rates up to 200MHz, circuits with over 50 different clock-regions, targeting European and Asia-Pacific processes down to 180nm.

For more information: Bart De Mey • Bart.DeMey@imec.be • Tel: +32 16 281 249 • http://www.imec.be/mtc/

Industry link

IMEC member of the OFDM Alliance

The OFDM Alliance was set up under strong impulse of Wi-LAN Inc. and Philips Semiconductors. It is a voluntary association of hardware manufacturers, software firms and other users of orthogonal frequency division multiplexing (OFDM) technology in wireless applications. The OFDM Alliance was created to foster a single, compatible OFDM standard, needed to implement cost-effective, high-speed wireless networks on a variety of devices. OFDM is a cornerstone technology for next generation of high-speed wireless data products and services for both corporate and consumer use. With the introduction of the IEEE802.11a, ETSI Hiperlan/2 standards, and multimedia applications, the wireless world is ready for products based on OFDM technology.

IMEC is member of the OFDM Alliance and has presented its OFDM technology under great interest. To date, IMEC is the only institute with ASICs for wireless in-door communication.

Awards

Patrick Schaumont received the VSIA Outstanding Contributor Award

The Virtual Socket Interface Alliance (VSIA) aims to dramatically accelerate system-chip development by specifying open standards that facilitate the mix and match of virtual components from multiple sources. VSIA members work together to solve the technical barriers to design integration of SoCs (system-on-chip). Since 1999, Patrick Schaumont (researcher at IMEC's DESICS division) is member of the VSIA SLD (System Level Design) group. He contributed to the system level behavioral interface documentation standard (SLIF) by means of a pilot project. This pilot project demonstrated the practical application of the standard, and resulted in a reference example section included in the released standard. For this work, Schaumont received the VSIA outstanding contributor award at last Design Automation Conference.

Recently, IMEC became member of VSIA. As center of excellence in SoC design, IMEC wants to actively contribute to state-of-the-art, industry-strength standardization and transfer techniques of virtual components. As a result, also IMEC's research partners will benefit from the in-house standardization expertise that is created out of this effort.

Events

IFST 2001 - Fourth international forum on semiconductor technology

March 7-8, 2001, Antwerp, Belgium

The IFST symposium is designed to bring together scientists and business people from around the world, to discuss advances in semiconductor technology, focussing on international collaborations, and more specifically emphasizing issues related to the famous international technology roadmap for semiconductors (ITRS). It is sponsored by a variety of semiconductor consortia and industry organizations. In 2001, the IFST symposium will come to Europe for the first time, and will be organized by IMEC, with the help of various international consortia such as ASET, COSAR, International SEMATECH, MEDEA, SELETE, SRC, and others.

Following a plenary session, there are 5 technical sessions on advanced lithography (157nm optical and next-generation lithography), 300mm fabs and fab productivity, ES&H (environment, safety & health) and full-cycle analysis, limitations faced by the roadmap (the so-called “red brick wall”), and finally a panel discussion.

The IFST meeting will immediately follow the SEMI Industry Strategy Symposium (March 5-6, at the same location).

Calendar

Upcoming conferences, workshops, symposia

International forum on semiconductor technology (IFST 2001)	March 7-8, 2001	Antwerp, Belgium
EUROSIME conference	April 9-11, 2001	Paris, France
International symposium on VLSI technology, systems and applications (2001 VLSI-TSA)	April 18-20, 2001	Taiwan
International workshop on information processing in cells and tissues (IPCAT'2001)	August 13-17, 2001	Leuven, Belgium

For more information: http://www.imec.be/6/6.html

Patents

Europe

Method for programming a semiconductor memory device. (EP 0740306)

US

Method and device for measuring the charge carrier distribution in a semiconductor element. (US 6091248)
Low temperature adhesion bonding method for composite substrates. (US 6093577)
Fully overlapped nitride-etch defined device and processing sequence. (US 6071825)
Control flow optimization for fast system simulation and hardware/software storage minimization. (US 66064819)

Japan

Method and apparatus for resistance measurements on a semiconductor element. (JP 3069129)

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Request for more information

nº 28 October 2000 imec newsletter

I want to receive more information on:

- ❑ IMEC's OFDM technology
- ❑ SoC++ design environment
- ❑ Hybrid integration of thinned metamorphic HEMTS on germanium
- ❑ IMEC's industrial affiliation programs on .....
- ❑ Other: .....

Please put me (or my colleague) on your mailing list for following publications:

❑ IMEC scientific report ❑ IMEC annual report ❑ IMEC newsletter

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