imec newsletter

IMEC, Kapeldreef 75, B-3001 Leuven, Belgium no 25 - October 1999

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Annual Research Review Meeting '99

World's first OFDM modem in silicon for wireless indoor communication networks

The OFDM-modem chip, developed in collaboration with SAIT, was processed and fully tested on a PCB.

Mobile and cordless voice communication have become a commodity over the last few years. In the meantime, broadband data communication has emerged fueled by the success of the Internet. Most of this communication is taking place through wirelines such as twisted pair and coax.

OFDM-modem development board.

However, broadband wireless solutions such as wireless local area networks, wireless domestic networks and wireless local loops are on their way.

Already, the IEEE802.11a and ETSI Hiperlan-II committees have drafted standards for broadband multimedia indoor communica-

continued p.2

ARRM 99

In this issue...

World's first OFDM modem... 1
Wavelength and mode stabilization... 1
Editorial 2
Dummy-free STI concept... 3
Single-package wireless transceiver design 4
Release of Atomium 1.1 5
Efficient high-level simulation... 6
GSM-based position location and tracking 6
Parallel optical interconnection ... 7
US office 8
New project to develop 100-nm CMOS... 8
New spin-off 9
DSP-office in FLV 10
Events 11
Patents 11
Colofon + Reply card 12

Wavelength and mode stabilization of widely tunable lasers for WDM systems

A new control scheme has been developed that allows to maintain a stable operation of widely tunable laser diodes for optical fiber networks.

Wavelength division multiplexing (WDM) techniques are being introduced in optical fiber networks at a rapid pace. While today's commercial systems are based on groups of constant wavelength distributed feedback (DFB) laser diodes, it is expected that in future systems wavelength tunable laser diodes will become key components. In particular widely tunable laser diodes – diodes that can be tuned over the complete wavelength range (about 50 nm around 1550 nm) of the Erbium Doped Fiber Amplifier (EDFA) – will become indispensable. These are devices with a 4-section optical cavity in which 4 analog electrical currents are needed to control the operation.

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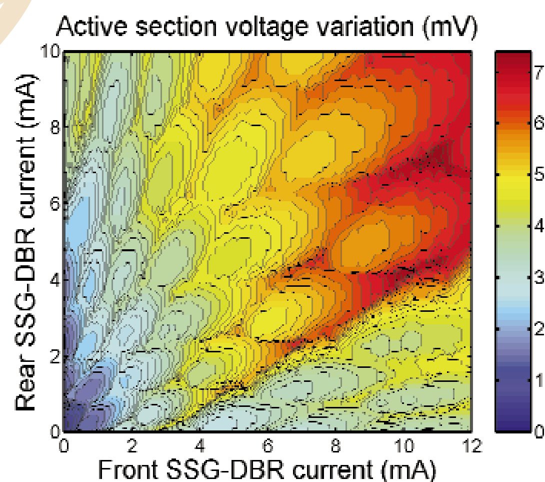


Fig. 1: Voltage across the gain section vs. the two grating currents; the minima correspond to stable monomode behavior.

Editorial

Ready to step into the next millennium

Another year has passed by since the last Annual Research Review Meeting. The industry's face has changed from a rather bad situation to a genuine recovery. Started in the first quarter of this year, semiconductor sales are showing robust growth. PC units sales are remaining strong and driving higher microprocessor sales. Meanwhile, new market drivers are gradually taking over from the PC dominancy, such as Internet appliances, communications and automotive electronics.
IMEC hardly suffered from the crisis. In 1998, its contract research income even rose by 10% indicating that more than ever, industry recognizes the need for independent R&D centers as strategic technology partner, based on early insight and risk & cost sharing.
This year's ARRM again reflects IMEC's latest progress in R&D, from deep-submicron process technology to advanced system-on-chip design. We had a first look. Development of advanced deep-submicron process modules has switched to another higher gear by the installation at IMEC of one of the first full-field 193-nm step & scan systems, ASML's PAS5500/900. At the same time a new initiative was launched this summer to develop 100-nm CMOS technology. Copper interconnects were successfully integrated in a dual damascene architecture with low-k dielectric material. Research in reliability resulted in the fact that scaling the gate oxide thickness to a few nanometers will lead to marginal intrinsic reliability, limiting the downscaling of CMOS technologies. Therefore, research was conducted on high-k materials for new gate dielectrics such as Si_3N_4 and Ta_2O_5. Future systems-on-a-chip need to be designed and developed for applications that will be at the cross-road of communications, computers and consumer electronics. This evolution towards single-chip systems requires a highly-advanced systematic design methodology supported by data models, architectures, libraries and CAD tools. At IMEC, research focuses on these challenges. Examples include the C++ design environment with the OCAPI library, and TIPSY, a design environment that supports executable system specification. TIPSY has been applied as demonstrator for an ADSL modem. Other results include the work on power optimization through memory management, an OFDM modem for wireless communication and an MPEG-4 chip. For some applications such as RF telecom systems, single-chip solutions might not be the right choice and systems-on-a-package have therefore been investigated, based on IMEC's thin-film multi-chip module technology.
A new item at the ARRM is the issue of training. In 1999, a new strategic training initiative was launched to concentrate and expand IMEC's activities in training for the semiconductor industry. In the past year, no less than 1,100 participants were enrolled, from process operators and technicians over process- and design engineers to non-technical professionals from industry.
It has been an exciting year since last ARRM, and at the eve of the new millennium, IMEC is ready to take up the new challenges.

Jan Wauters

continued from p.1

tion in the 5 GHz band based on orthogonal frequency division multiplex (OFDM) communication.
IMEC is developing the next generation OFDM-based wireless communication systems. The goal is to achieve an overall network capacity of 155 Mbit/s. To reduce system cost and power consumption, the entire modem is integrated into a single package. This year, the baseband ASIC was designed, integrating the entire OFDM functionality. It allows great flexibility for optimizing the functional parameters such as FFT length, spreading factor, and length of the guard interval towards a specific scenario such as 802.11a or Hiperlan-II.
Furthermore, new DSP algorithms were established that improve bandwidth and power efficiency. Adaptive loading is used to suppress narrowband interference and to overcome frequency selective fading. The bandwidth efficiency is enhanced by antenna array processing. Each of these antennas provide signals that can be combined on a per carrier basis after the OFDM demodulation. This allows to have a considerable performance gain, while keeping the algorithmic complexity within limits.

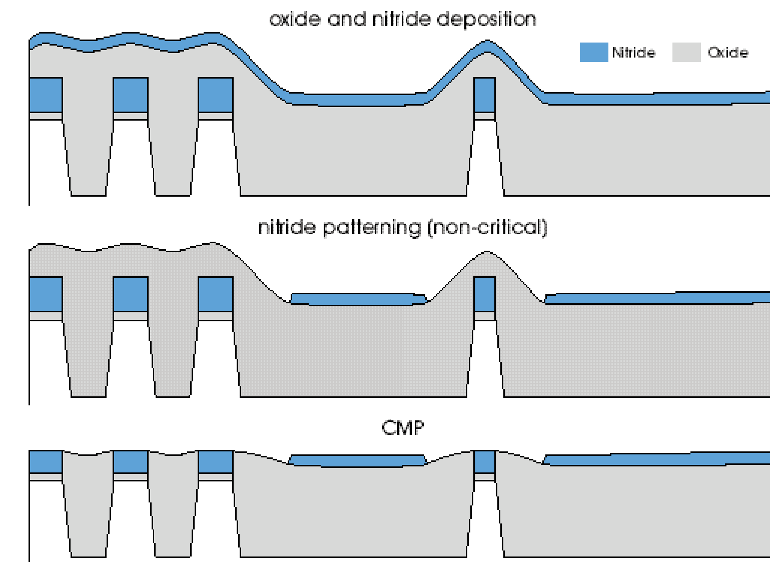
Dummy-free STI concept for mixed-signal applications

A new shallow trench isolation (STI) module was developed to solve the problems related to dummy active areas when used in mixed-signal technologies.

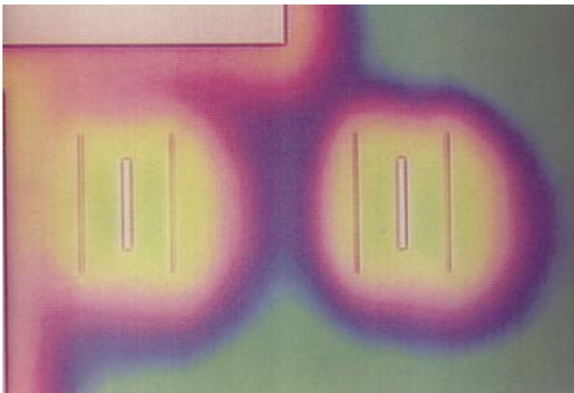
STI is becoming the mainstream lateral isolation module for deep-submicron technologies. However, it has the drawback that it requires dummy active areas due to the limited within-chip uniformity with the chemical mechanical polishing (CMP) step. These dummy active areas can cause severe problems in mixed-signal analog/digital applications due to the increased capacitive coupling and associated noise.

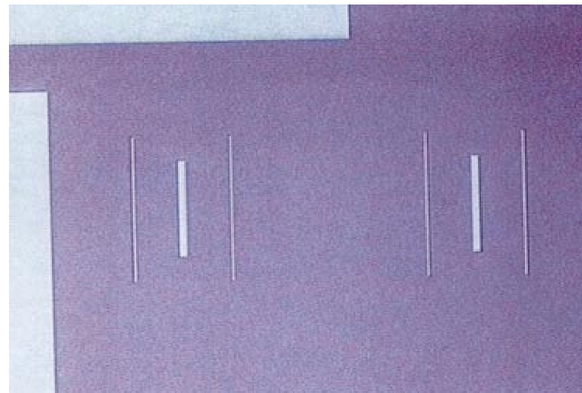
The new STI module ensures minimum oxide dishing and nitride erosion without the need for dummy active areas. The approach consists of implementing a nitride protective layer on top of the field region. A slurry with high selectivity towards nitride should be used to obtain optimal results. In this way, dishing of field oxide and erosion of isolated active regions is effectively eliminated.

The new STI approach has been successfully implemented in a 0.18-µm CMOS process flow with 3.5-nm gate oxide thickness. Experiments showed that gate oxide quality is not degraded at the isolation edges, and very low defectivity levels are related to the STI module. The success for the approach is also confirmed by the limited threshold voltage difference between dense and isolated transistors of 20 mV, and the fact that no subthreshold hump was observed.



Process flow of the new STI module. After trench filling with HDP oxide, a second nitride layer is deposited and patterned so that a protective nitride layer is left on wide field regions.





Top view micrographs showing isolated active area regions surrounded by large field areas after CMP, using a standard STI process flow (left) and the new dummy-free approach (right).

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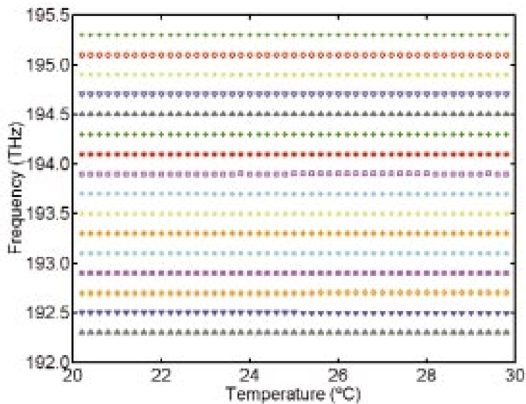


Fig. 2: Variations in frequency for a temperature variation between 20 and 30°C for 16 ITU channels.

Since years, IMEC's associated laboratory, INTEC at the University of Gent, has been doing research on designs of such devices to optimize their performance. One of these designs – the so called GCSR-laser – is now being commercialized under license contract by the Swedish company Altitun AB. Now research is focused on the control algorithms needed to manage these complex devices. A new control scheme has been developed that allows to maintain a stable operation (stable power, wavelength and side mode suppression) of widely tunable laser diodes. At the same time, the scheme can be used to increase the speed with which a look-up table can be created for the selection of the different wavelength channels.

The control scheme is a feedback based scheme that generates corrections to the tuning currents based on measurements of the wavelength and of the voltage across the gain section (one of the 4 sections in a widely tunable laser). Optimum operation points always correspond with minimum mirror losses and hence minimum voltage across the gain (or active) section *(see Figure 1)* and hence two tuning currents are set by the requirement of minimum voltage. This is achieved by adding small-signal, low-frequency modulations to the currents and measuring the small-signal voltage modulation with lock-in amplifiers. A third tuning current, for the phase section, is derived from the wavelength measurement using a wavelength locker (or periodic optical filter). The efficiency of the method is illustrated by the very small frequency variations (< 0.5 GHz) that result when the stabilization is applied, even when the temperature is varied over 10 °C *(see Figure 2)*. The method is also more generally applicable than other, previously reported stabilization methods.

This new control scheme was demonstrated on widely tunable lasers produced by NTT (Japan) during the recently held European Conference on Optical Communication (ECOC) in Nice. The demonstration set-up will also be displayed at the Annual Research Review Meeting.

For more information, please contact

G. Sarlet (INTEC):
Tel. +32 9 264 89 30
G. Morthier (INTEC):
Tel. +32 9 264 89 34
R. Baets (INTEC):
Tel. +32 9 264 33 29

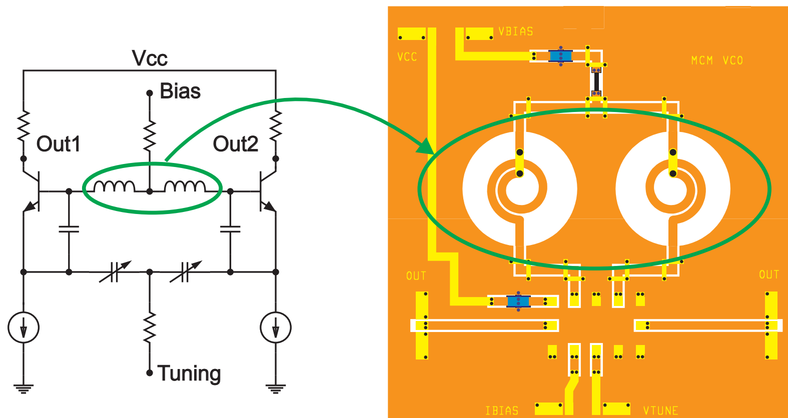
Technology report

Single-package wireless transceiver design

The realization of a 5 GHz receiver front-end module for WLAN demonstrates the possibilities of system-on-package solutions.

High-performance wireless applications require low power consumption and high degree of integration. For some applications (e.g. WLAN), a single-chip solution for the analog front-ends is not feasible. At IMEC, the single-package integration of complete transceivers is investigated based on a thin-film multi-chip-module technology (MCM-D) with integrated passives. The MCM substrate is a common carrier onto which different ICs and microelectro-mechanical systems (MEMS) are mounted with a flip-chip technique to reduce signal degradation due to bondwire parasitics. Passive components such as RF bandpass filters, inductors, capacitors and resistors are directly integrated into the MCM substrate with the use of the multi-layer structure of the MCM-D technology. The quality factors of the passive components are very high, especially compared to on-chip passive components. As an example, a 1.4 nH inductor has a measured maximum Q of 82 at 8 GHz. This is much higher than in a CMOS technology, even with copper and low-k dielectrics, where Q's up to 22 are reported for similar inductances. Even the integration of the antenna in this MCM-D technolo-

gy has been demonstrated. In this way, this technology is suitable for a complete system integration of a transceiver, from the antenna to the digital baseband circuitry. To demonstrate the approach an MCM is being fabricated that contains a 5 GHz receiver front-end for WLAN. This front-end includes the RF blocks and two RF band-pass filters. The voltage-controlled oscillator in this front-end is shown in the figure below. The phase noise of the oscillator or its power consumption can be kept low if the elements of the LC tank have a high quality factor. This is obtained by implementing the inductor on the MCM substrate. This example shows that chip-package co-design leads to a performance improvement or a power consumption reduction. By a careful co-design of the RF front-end from the architectural level, the improvements are even more drastic than with trade-offs at the circuit level only.



Voltage-controlled oscillator in a 5 GHz receiver front-end for WLAN.

Technology report

Release of Atomium 1.1

For multimedia applications, the manipulation of data has a major or even dominant effect on the cost of the global system. This is mainly due to the large impact of power and area of the memory organization and global data transfer between system components. To address this, IMEC has previously developed a data transfer and storage exploration (DTSE) methodology that has proven itself in the context of multimedia system design.

The methodology does, however, require both an in-depth analysis and extensive transformations of the application's program code. Applying it without the assistance of CAD support can therefore be very tedious, error prone, and time consuming, even for applications of modest size. This is being addressed by the Atomium (A Toolbox for Optimising Memory I/O Using geometrical Models) project. The goal of the project is to provide the designers with a CAD environment that drastically simplifies the application of the most important steps of the DTSE methodology.

Recently, an Atomium re-engineering action was initiated. The overall objective is to properly implement (a subset of) the DTSE methodology to overcome the need for inside knowledge and manual tuning by the Atomium developers.

The input for the Atomium CAD environment is a specification of the application at the behavioral level, expressed in a (large) subset of the ANSI-C programming language. The output is a transformed description, functionally equivalent to the original one, but typically leading to strongly reduced memory size and power consumption requirements when fed into traditional high-level synthesis tools.

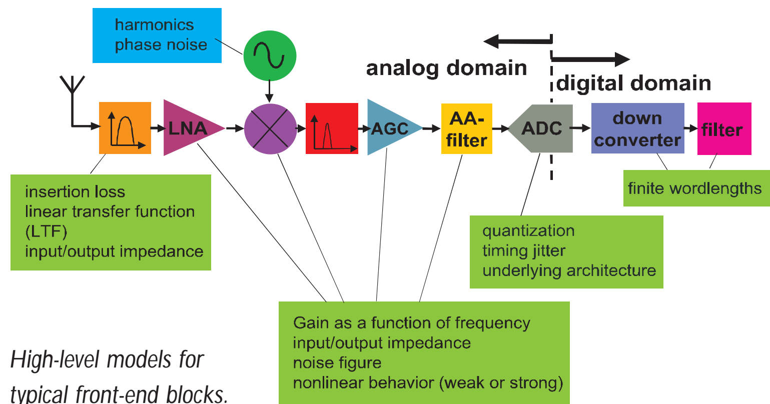
Application targets include real time multimedia, wireless and wired communication terminals that handle complex arrays, and sophisticated protocol processing, which handle large sets of records organized in tables and pointers. The novel design technology allows a major and proven impact on the product cost.

Using ATOMIUM, IMEC has designed for instance a custom memory architecture for scalable MPEG-4 texture compression, that reduces the required memory size by a factor of 10 compared to a straight-forward implementation, enabling a low power implementation.

Efficient high-level simulation of mixed-signal front-ends

A high-level simulator, FAST, is developed to perform simulations of front-end architectures of wireless transceivers.

For the development and exploration of new architectures, simulation before the actual realization is very important. Such simulations require that the architectures are described at a high level of abstraction. In this way, end-to-end simulations of a complete telecom link are possible and the performance of this link (e.g. in terms of the bit-error-rate) can be simulated with the inclusion of the signal degradation caused by the front-end blocks.
To this purpose, the high-level simulator FAST (Front-end Architecture Simulator for Telecom applications) is developed at IMEC. For simulation with FAST, a front-end architecture is described in C++. This description contains a high-level model for each front-end block, as well as the connectivity of the different blocks. The figure illustrates the high-level models for some typical front-end blocks.



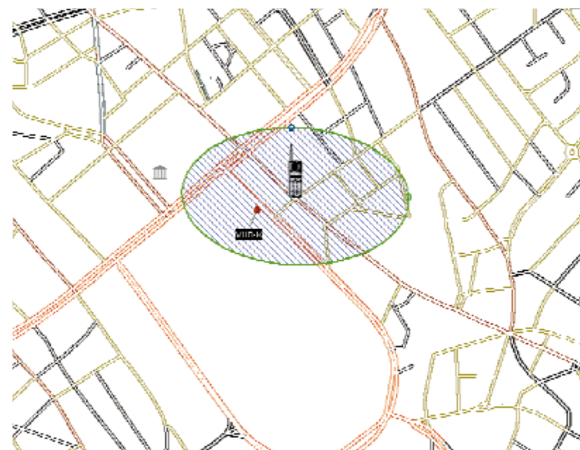
High-level models for typical front-end blocks.

Prior to simulation the high-level C++ description is translated into a multi-rate multi-carrier dataflow model: RF signals, which are usually bandpass signals are represented by a complex modulation around a carrier. By shifting these carriers and their harmonics to DC, a set of equivalent low-pass signals are obtained, which can be processed efficiently during simulations. Both the carrier frequencies of the equivalent low-pass signals and the simulation timestep is automatically changed throughout the architecture. This leads to a high simulation efficiency compared to traditional approaches, that use one single timestep for the complete simulation in which all carrier frequencies are present everywhere in the front-end.

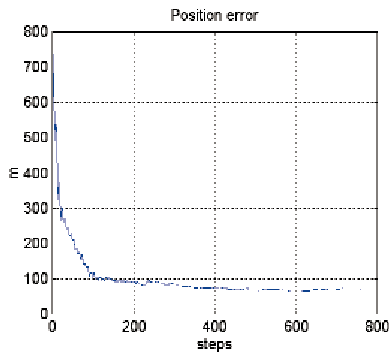
GSM-based position location and tracking

A Mobile Station localization system has been developed by IMEC's associated laboratory ETRO at the University of Brussels (VUB) using wireless cellular communication, i.e. the Global System for Mobile communications (GSM). It was first announced in the IMEC Newsletter of November 1998; here are some extra details.

IMEC/ETRO continues its research on the development of a localization system based on wireless cellular networks. This research work started in the framework of a particular automotive application in a project of IMEC/ETRO and Smart-Move, a company specialized in vehicle telematics. Basic positioning algorithms using timing advance measurements were elaborated during this phase. Moreover, a road network database along with fast access and spatial query routines were implemented to improve the positioning accuracy by involving map matching and tracking techniques. Now, the focus is on the refinement of the positioning algorithms (mainly speed and accura-



Graphical representation of the positioning results for a static mobile station. The localization test was performed in building K, Campus VUB.



Position accuracy (expressed in meter), as a function of the number of timing advance parameter acquisitions.

cy) for still and moving mobile stations, using timing advance and signal strength measurements, in an effort to exploit the current capabilities of the GSM, without modifying the GSM infrastructure. Figure 1 shows the estimated position (phone icon), of a stationary mobile station (red dot). The position error is 180 m. The error ellipse (300 m x 200 m) indicates the area where the mobile station is likely to be located. *Figure 2* presents the results of the position accuracy refinement algorithm applied to a static mobile station.

IMEC/ETRO is currently looking for industrial collaboration, in various application domains.

For more information:
Hichem Sahli
VUB (ETRO)
Pleinlaan 2, B-1050 Brussel
Tel.: +32 2 629 29 16
Fax: +32 2 629 28 83
Email: hsahli@etro.vub.ac.be

Technology report

Parallel optical interconnection between CMOS- ICs using arrays of micro-cavity light-emitting diodes and plastic optical fibers (POF)

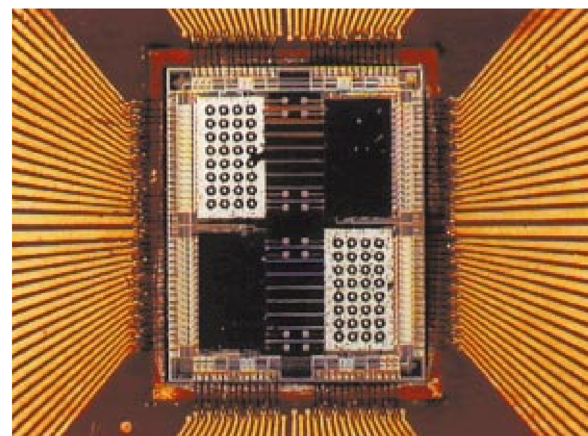
A direct optical interconnection from CMOS to CMOS via optoelectronic components and an optical pathway has now been demonstrated.

In the past years, IMEC's associated laboratory, INTEC at University of Gent, has made considerable progress to develop arrays of micro-cavity LEDs (MC-LED) with high power conversion efficiency and modulation speed. These robust and easy-to-fabricate devices are based on quantum-well active layers embedded in a wavelength-scale optical cavity. They can be optimized for coupling a large fraction of output light into the limited numerical aperture of a lens or of an optical fiber.

A potentially important application is to use them in parallel optical data links. Arrays of MCLEDs (as well as VCSELs, vertical cavity surface emitting laser) are used to demonstrate inter-chip, intra chip and intra-board optical interconnect. This work is performed in collaboration with ELIS, another associated laboratory of IMEC at the University of Gent, and IMEC's Novel Materials and Components Group.

A direct optical interconnection from CMOS to CMOS via optoelectronic components and an optical pathway has now been demonstrated. The CMOS ICs contain drivers and receivers that convert the digital signals into analog signals and vice versa. The LED-array chip (and also the detector-array chip) is flip-chip mounted onto the CMOS chip allowing to implement an area interconnection. The light path consists of a custom made 2D ribbon of plastic optical fiber. This plastic optical fiber has an outer diameter of 125 µm, enabling a component pitch of 250 µm. Successful digital information transfer was achieved with drive currents of 2 mA for the LEDs.

Work is continuing to improve the performance of these parallel optical links in terms of speed and power dissipation. The LEDs can be operated at data rates of 1 Gb/s when driven from a dedicated drive circuit. Work is on-going to develop advanced CMOS drivers that achieve this task. In parallel with this a relatively large-scale optically interconnected FPGA demonstration system is being developed in collaboration with ELIS.



Top view of a packaged CMOS chip with 2 LED arrays (dark areas) and 2 detector arrays (brighter areas) hybridized on top (picture courtesy GMMT).

For more information, contact:
Roel Baets, INTEC
Roel.baets@intec.rug.ac.be
+32 9 264 33 16

IMEC opens an Office in the US

A considerable amount of our annual income from international contract research is from collaboration with US companies and industry partners. This makes the US an important business region with a lot of opportunities for IMEC. In addition, the heart of the semiconductor industry, Silicon Valley, has the highest concentration of integrated device manufacturers, materials suppliers and equipment vendors for the semiconductor industry. With all this in mind, IMEC decided to open up an office in Silicon Valley to have a permanent representation in the US. This way we strengthen our services to our partners in the United States and it also allows us to closely follow what's happening in the semiconductor market which is characterized by ever changing market dynamics and in full flux.

On July 8 we held an open house were the invited guests could meet with the new US staff and some of our European executives. We had about 30 people visiting the office that day. The atmosphere was very informal and we had a lot of stimulating discussions and interactions.

New project to develop 100-nm CMOS technology

The initiative is in response to new schedules to be published in the 1999 International Technology Roadmap for Semiconductors. This predicts the introduction of 0.13 micrometer CMOS by 2001 and 100 nm by 2003, two years earlier than forecast in last year's SIA roadmap. If these targets are to be achieved, early investigation and evaluation of specific process modules and the development of innovative device and process integration concepts are urgently required. IMEC is therefore calling for industry collaboration in a major R&D effort to develop the 100 nm generation node, where major technological bottlenecks are expected.

IMEC's 100 nm CMOS technology project will concentrate on optical lithography, advanced etching techniques, new gate stacks, ultra-shallow junction formation, transistor architecture improvements, back-end architecture and study of the technological limits in terms of reliability.

Participation in the project is available through the IMEC Industrial Affiliation Program (IIAP) or via bilateral contracts for the development of specific process modules or of overall process integration and device architecture concepts. IMEC is also forming a European consortium to address aspects of the activity, for which it has requested funding support from the European Commission.

Industry link

Extending optical lithography to its limits

The 193 nm litho cell (ASML PAS5500 / 900 ArF Step & Scan system interfaced to the TEL Act 8 coat and development track), fully operational since end of July in IMEC, is the workhorse of IMEC's Industrial Affiliation Program on 193 nm lithography process development, counting over 25 IC manufacturers, equipment and material suppliers. Meanwhile, IMEC co-operates with ASML to develop the next generation deep UV-lithography, using 157 nm wavelength.

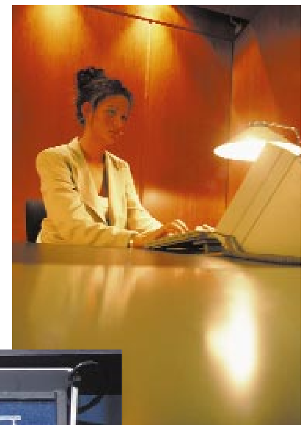
Focus on Flanders

New IMEC spin-off company

This new engineering and project development firm, a joint venture with the company Ecofys from the Netherlands, is targeted towards the development of innovative energy systems and products, and their high-quality and economically feasible applications. The initiative originates from three engineers who were active in the field of renewable energy for almost 10 years, and who have acquired considerable experience in research, development and management. The company's differentiator when compared to existing study bureaus is their independent character both from energy companies, as well as from renewable energy technologies suppliers. In addition, they can act as an independent consulting bureau for governmental services.
The company's headquarters are based in Brussels (Belgium).

Their activities include research, product development, technical and strategic consulting in:

- Photovoltaic solar energy
- Solar thermal energy
- Wind energy
- Energy in buildings
- Renewable energy supply
- Energy & Environment



For more information, contact
Geert Palmers, 3E
Eredienststraat 7/19
B-1000 Brussel
or send an e-mail to info@3e.be

IMEC brings DSP expertise to Flanders Language Valley

In September 1998, IMEC joined Flanders Language Valley (FLV), the regional cluster on speech processing, initiated by world-famous Lernout&Hauspie Speech Products. Two months ago, IMEC opened its office on the premises of FLV. The office will enable FLV companies to exploit IMEC's expertise on digital signal processing (DSP) for their new product developments in the field of speech and language technologies.

A view on FLANDERS LANGUAGE VALLEY

FLV stands out as a unique breeding ground for the development and commercialization of speech and language technology based products and services.
Lernout&Hauspie Speech Products, in the very proximity of FLV, supplies the FLV companies with advanced core technologies such as automatic speech recognition, text-to-speech, text-to-text and digital speech compression. To date, FLV counts over 26 high-tech companies and over 100 additional companies are expected to join, endorsing Flanders Language Valley as a worldwide center of expertise in speech and language technologies and artificial intelligence.
The heart of Flanders Language Valley is situated within FLV Campus, a 65-acre business park, which is being built in Ieper, in the Flemish region of Belgium. FLV aims to exploit some strong assets, notably the availability of top multilingual speech engineers and linguists, proximity to Lernout & Hauspie Speech Products, venture capital focused on speech and language related technology applications provided by FLV Fund (67 million USD), business support and incubation services and proximity to European cities and universities. Members of FLV Fund include Microsoft and Intel.

DSP expertise at IMEC

One of the fastest expanding segments in the electronics industry is with no doubt DSP. The digital signal processing market has been growing with an astonishing 39% over the past 10 years. Owing to the very large scale integration in microelectronics, DSP has been able to invade almost any technology market in which traditional analog electronics were prevalent, such as image processing, multimedia, set-top boxes, GSM, PABXs, cable-TV modems, audio processing (CD, equalizers,...), etc. In the development of speech and language technologies, DSP is of the utmost importance. With the ever increasing computational power of miniaturized electronics circuits, DSP has succeeded in boosting the field of speech technology.
Since its foundation in 1984 IMEC has built up a great tradition in DSP. IMEC has implemented DSP technologies in applications in the fields of telecommunication and multimedia. DSP is the cornerstone of the IMEC spin-off companies Sirius Communications, Target Compiler Technology, EASICS, Smartmove,… On a broader scale Flanders stands out for its remarkable concentration of high-tech companies in the field of DSP, personified by the DSP Valley consortium.

IMEC will operate in FLV from its office amid the FLV companies. It will assist FLV companies to take core speech technologies up to the application level by filling in the indispensable DSP layer. The permanent presence in FLV will also trigger cooperation with local SMEs in the region.

For more information:
IMEC office in FLV
Niek Van Dierdonck
Flanders Language Valley 44
B-8900 Ieper
+32 57 23 01 42

Flanders Language Valley
www.flv.be

The Good-Die International Workshop

Aix-en-Provence, France, May 22-24, 2000.

The GOOD-DIE International Workshop on Challenges for Advanced Semiconductor-die Technologies will present and explore the current issues and future trends for the use of unpackaged and minimally packaged semiconductor die, with or without connection structures, in electronic systems. The workshop will include keynote presentations and sessions with a wide range of topics including, but not limited to: wafer level packaging, wafer test and burn-in, defect-oriented testing methodologies for KGD, low cost flip-chip technologies, CSP trends, bare die handling and shipping, standards, die design data exchange issues, system applications of KGD infrastructure and equipment.

For more more information on the workshop
CAST 2000, Good-die Workshop
c/o IMEC vzw
MCP Division, Deboes Chantal
Kapeldreef 75, B-3001 Leuven,
Tel. : +32 16 28 12 81
Fax : +32 16 28 15 01
E-mail: deboes@imec.be
http://www.gooddie.net/gdimages/cast2000/cast1.htm

5th International Symposium on Ultra Clean Processing of Silicon Surfaces (UCPSS '99)

Oostende, Belgium, September 18-20, 2000.

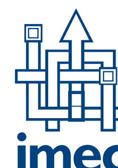
The conference, organized by IMEC, is intended to increase the level of understanding on ultra-clean processing technology in all steps of IC-production technology. Issues to be addressed cover a.o. general issues in ultra-clean technology, ultra-pure gases, chemicals, DI-water, chemical and physical cleaning in liquid or gaseous ambients, enhanced dry cleaning in integrated and UHV processing, application-specific cleans (oxidation, epitaxy, CVD, metallization, etc.), cleaning and surface treatments at the interconnect level, cleaning after Chemical-Mechanical-Polishing (CMP), dry-etch resist strip and polymer removal, contamination/particle control and its relation with process performance, process and contamination diagnostics, in-situ monitoring and process control, environmentally friendly technologies and mass balance equations, and many more. On September 17, a tutorial session will be organized on "Ultra-Clean Processing Technology and general cleaning issues".

For more information, please contact:
Marc Heyns, IMEC,
c/o Timshel Conference Service,
Roeselveld 7,
B-3020 Herent, Belgium
Tel. +32 16 29 05 10
Fax +32 16 29 00 10
E-mail info@timshel.be
http://www.imec.be/ucpss/UCPSS2000firstcall.html

Patents granted – 2nd Q & 3rd Q 1999

Europe	Resolution enhancing optical phase structure for a projection illumination system • EP 637393
Taiwan	Apparatus and method for wet cleaning of flat substrates in particular semiconductor wafers TW 099314
Japan	Method of fabricating optoelectronic components • JP 2905597
US	DRAM applications using Vertical MOSFET Devices • US 5914504
US	A method for processor modeling in code generation and instruction set simulation • US 5918035
US	Vertical Mosfet Devices, CMOS process integration, RAM applications • US 5920088
US	Method for semiconductor processing using mixtures of HF and carboxylic Acid • US 5922624
US	Pixel structure, image sensor using such pixel structure and corresponding peripheric circuitry US 5933190

Request for more information



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fax or send to: Marianne Van den Broeck, Public Relations Group, Business Development
IMEC, Kapeldreef 75, B-3001 Leuven, Belgium
tel. +32 16 28 14 91 fax +32 16 28 16 37

Publisher:

Prof. Gilbert Declerck, President
Editorial office: Jan Wauters & Olfa Marzouk
IMEC
Kapeldreef 75,
B-3001 Leuven, Belgium
Tel. + 32 16 28 16 87
Fax + 32 16 28 15 76
E-mail: Jan.Wauters@imec.be

Contributed to this number:

G. Badenes, R. Baets, I. Boerenkamp, J. Bormans, J. Cornelis, S. Donnay, R. Graulus, B. Gyselinckx, G. Morthier, G. Palmers, K. Ronse, G. Sarlet, N. Van Dierdonck, P. Wambacq, L.Vanwassenhove

USA contacts:

Rik Graulus and Kris Beyen,
IMEC, 960 Saratoga Ave, Suite 206, San Jose, CA 95129
Tel.: (408) 551 45 01
(408) 551 45 02
Fax: (408) 551 45 05
E-mail: graulus@imec.be
beyen@imec.be
http://www.imec.be/

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